AD-A045 589 RAYTHEON CO WAYLAND MASS ADVANCED DEVELOPMENT LAB F/G 17/9
R AND D EQUIPMENT INFORMATION REPORT. VOLUME I. WEATHER RADAR T--ETC(U)
APR 77 R K VANDERKRUIK, A J JAGODNIK F19628-76-C-0297

UNCLASSIFIED ER77-4128 AFGL-TR-77-0171 NL

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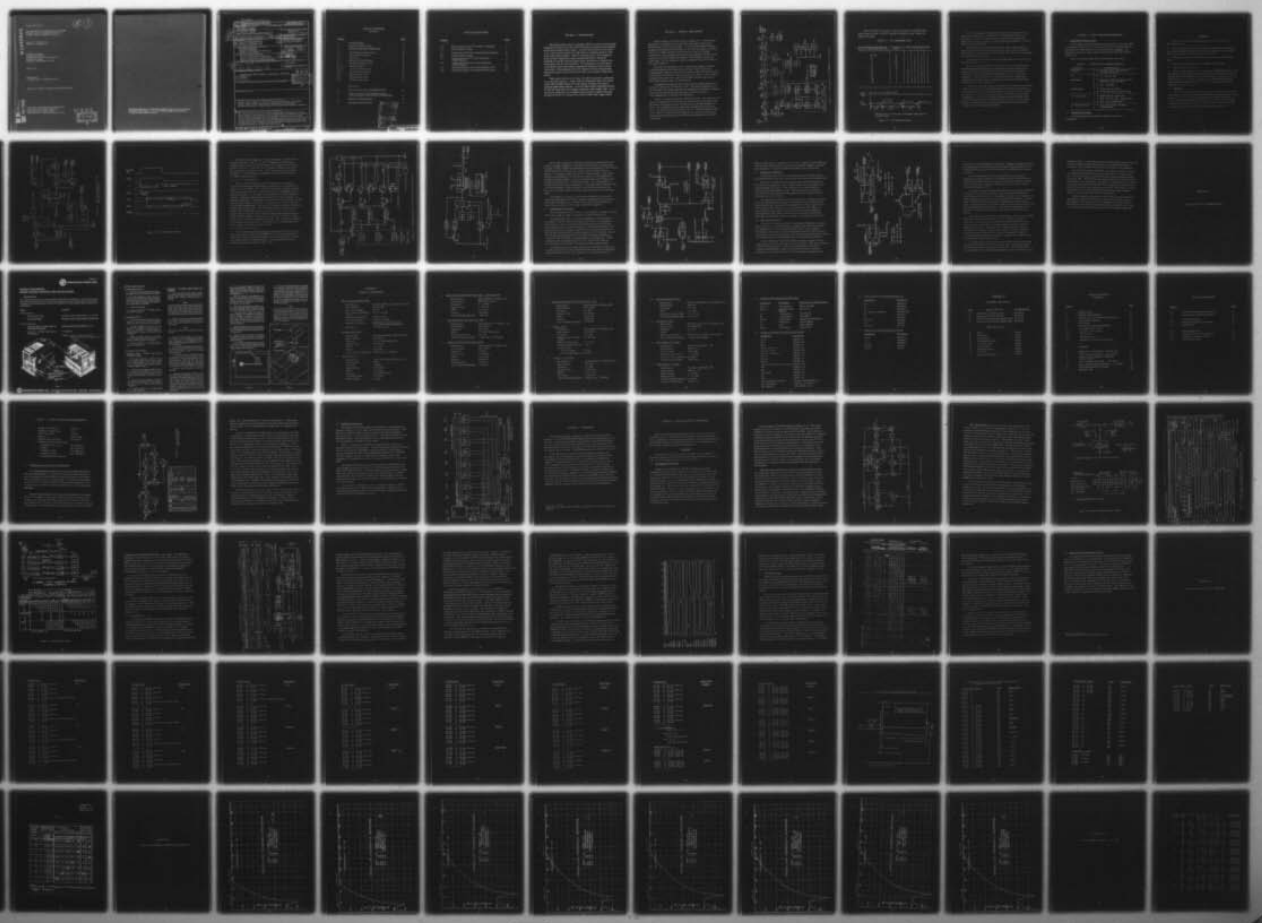

AFGL-TR-77-0171

R&D EQUIPMENT INFORMATION REPORT
Weather Radar Transponder (Volume 1)
Ground-Clutter Canceller (Volume 2)

Ronald K. VanderKruik
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Raytheon Company
Equipment Division
Advanced Development Laboratory
Boston Post Road
Wayland, Massachusetts 01778

April 1977

Final Report
1 October 1976 - 28 February 1977

Approved for public release; distribution unlimited

AIR FORCE GEOPHYSICS LABORATORY
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
HANSCOM AFB, MASSACHUSETTS 01731

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFGL-TR-77-0171
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): R and D Equipment Information Report. Volume I. Weather Radar Transponder. (Vol. 1) Volume II. Ground-Clutter Canceller. (Vol. 2)

5. TYPE OF REPORT & PERIOD COVERED: Final Report, 76 Oct. 1 - 77 Feb. 28

6. PERFORMING ORG. REPORT NUMBER: ER77-4128

7. AUTHOR(s): Ronald K. VanderKruik, Anthony J. Jagodnik, Jr.

8. CONTRACT OR GRANT NUMBER(s): F19628-76-C-0297

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Raytheon Company
Equipment Division
Advanced Development Laboratory
Wayland, MA 01778

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62101F; 66720601; 17 06

11. CONTROLLING OFFICE NAME AND ADDRESS
Air Force Geophysics Laboratory
Hanscom AFB, Massachusetts 01731
Monitor/Graham M. Armstrong/LYW

12. REPORT DATE: April 1977

13. NUMBER OF PAGES: 105

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Final rept. 1 Oct 76 - 28 Feb 77

15. SECURITY CLASS. (of this report): Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release; Distribution Unlimited

12 104p.

DDC RECEIVED OCT 27 1977 B

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)
Weather Radar Calibrator, Radar Performance Monitor, Transponder
Weather Radar Clutter Cancellation, Infinite Impulse Response
Sampled-Data Filters, Digital Signal Processing, Serial Digital Arithmetic

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)
This document describes two distinct equipments developed for use with meteorological radar systems. The Weather Radar Transponder calibrates a radar system in amplitude for both directions of travel from a remote location and additionally verifies its doppler response from an on-site location. The Ground Clutter Canceller removes unwanted ground returns and feed-through which would otherwise corrupt estimates of doppler spectral mean and width obtained by a Pulse-Pair Processor.

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Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

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SECTION I. INTRODUCTION

The Coded weather Radar Transponder (CRT) is a device which provides calibrated RF pulses to be used in the calibration of coherent and noncoherent E-band (old S-band) weather radars. It can be used at the site of the radar or at a remote location (where 115 VAC power is available) in the far field of the radar antenna pattern. When at a remote location, the transponder picks up radar transmission using a standard gain horn, detects the amplitude of each RF pulse and compares the amplitude to a standard level determined at the time of installation. The transponder then retransmits a noncoherent pulse-coded signal indicating the amplitude of the received radar pulse. The amplitude of the CRT response is known and alternates between two levels, one 20 dB below the other, every 1024 (or 2048) radar pulses.

When used at the site of the radar, the CRT can provide a calibration for a coherent processor. In this mode the transponder uses a CW sample of the radar STAMO instead of its own internal oscillator to produce a coherent coded signal response. A one-bit phase shifter alternates between 0° and 180° phase shift every trigger producing a fixed doppler shift. As in the off-site application, the amplitude of the coherent response alternates between two levels 20 dB apart every 1024 (or 2048) radar trigger pulses.

SECTION 2. GENERAL DESCRIPTION

A block diagram of the CRT is given in Figure 2-1. In the far field application, a waveguide horn receives the radar signal which is then directed to the CRT via coaxial cable. A circulator directs the RF pulse through some attenuation to the detector. The detected signal is amplified and fed to a sample-and-hold circuit and then to a set of 16 voltage comparators. Each voltage comparator has an adjustable reference which enables the set to be calibrated to indicate 1 dB increments in received power level. The 16 comparator outputs are encoded into a 4-bit word as indicated in Table 2-1.

The 4-bit word therefore covers a power level range of -12 dB to +3 dB with respect to the initial reference level. This 4-bit word is combined with a single reference bit to produce a 5-bit word which controls an RF switch and produces a coded group of up to 5 pulses. The reference bit indicates the start of the code and is present whenever the received power level is greater than -12 dB reference.

An additional comparator has a reference level midway between the number 13 and number 14 reference levels. Upon initial installation, in the test mode, the variable attenuator preceding the RF detector is adjusted to just activate this comparator and light a front panel indicator. This establishes the 0 dB power level reference.

Figure 2-2 shows the response timing of the CRT. The coded group of pulses are repeated up to three times for each received radar pulse, with the start of each group variable and determined by decade switches on a panel. T1 is adjustable in 10 μs steps with a potentiometer fine tune of 10 μs. T2 and T3 each are increments of 10 μs. The pulse width is either 2.0 μs every 4.0 μs for all three groups or is 2.0 μs for the first group, 4.0 μs for the second and 8.0 μs for the third as determined by a switch on the card.

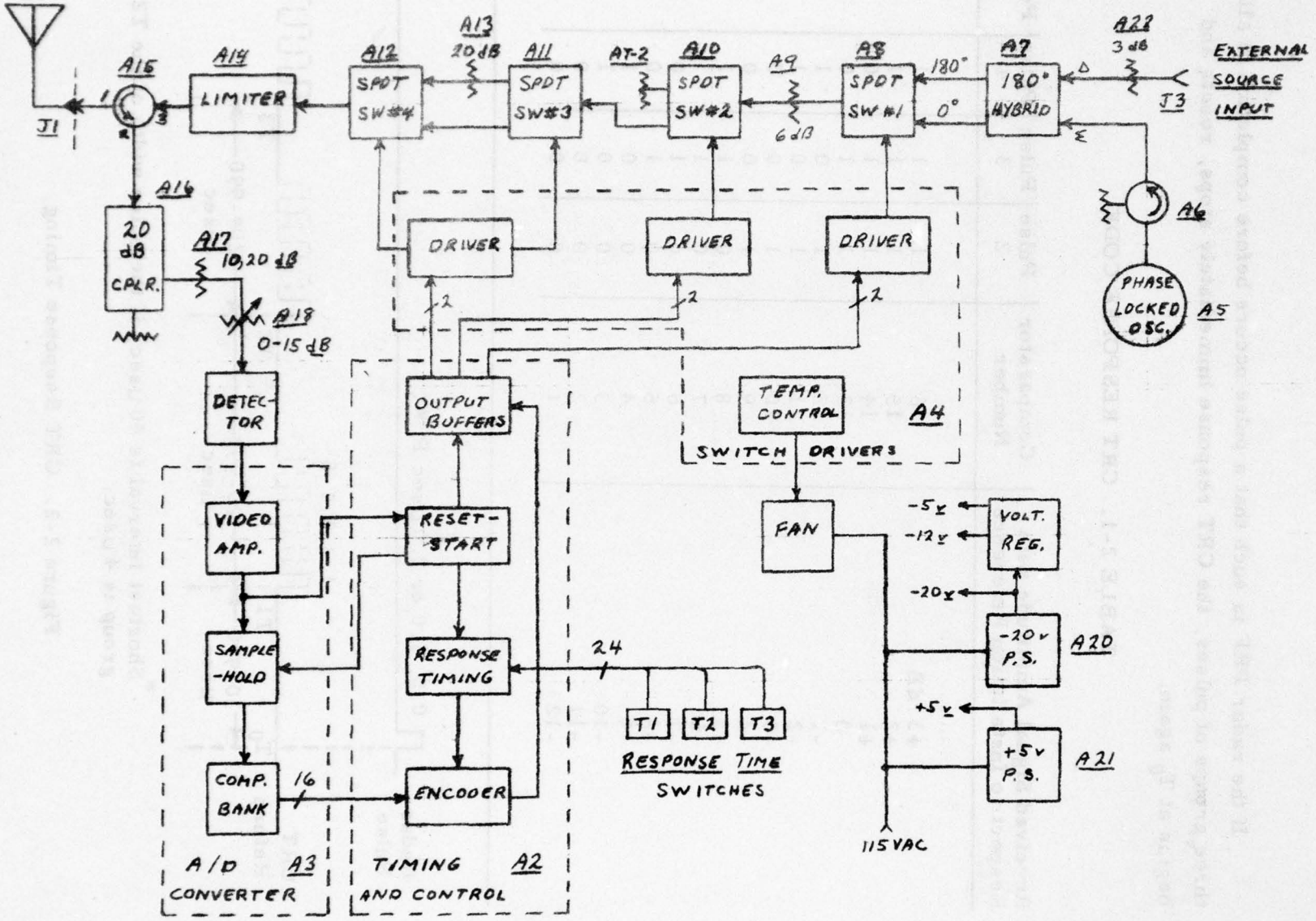
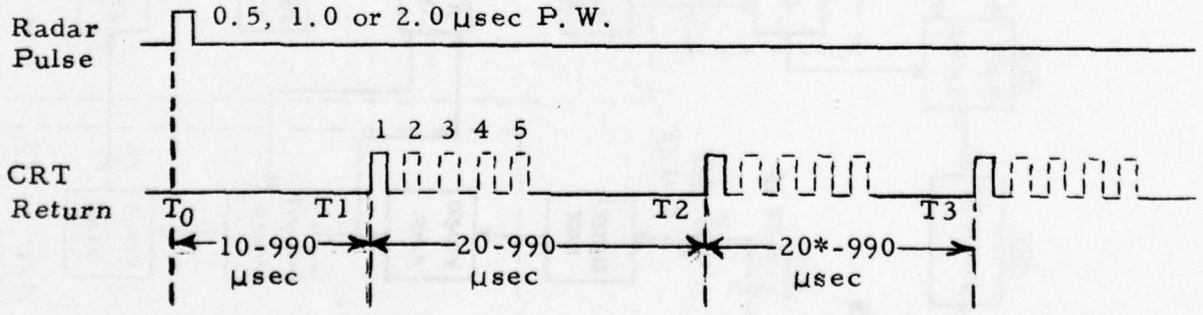


Figure 2-1. Block Diagram of the **Coded** Radar Transponder

If the radar PRF is such that a pulse occurs before completion of all three groups of pulses, the CRT response immediately stops, resets and begins at T_0 again.

TABLE 2-1. CRT RESPONSE CODE

Received Signal Amplitude with Respect to Installation Reference	Comparator Number	Pulse 2	Pulse 3	Pulse 4	Pulse 5
+3 dB	16	1	1	1	1
+2	15	1	1	1	0
+1	14	1	1	0	1
0	13	1	1	0	0
-1	12	1	0	1	1
-2	11	1	0	1	0
-3	10	1	0	0	1
-4	9	1	0	0	0
-5	8	0	1	1	1
-6	7	0	1	1	0
-7	6	0	1	0	1
-8	5	0	1	0	0
-9	4	0	0	1	1
-10	3	0	0	1	0
-11	2	0	0	0	1
-12	1	0	0	0	0



*Shortest interval is 40 µsec, if the pulse width of the T2 group is 4 µsec.

Figure 2-2. CRT Response Timing

The CRT response is derived from a crystal-controlled oscillator at exactly the same frequency as the radar. RF switch A10 (Figure 2-1) is controlled by the 5-bit word (translated to serial form) to produce the pulse-coded response; a digital '1' means a pulse is transmitted, a digital '0' means no pulse transmitted.

RF switches A11 and A12 provide the two levels of CRT response. Both switches are in one state (no loss line) for 1024 or 2048 radar pulses (determined by a switch on board), then switch to the other state (-20 dB line) for an equal number of pulses.

RF switch A8 is not used in the remote application and remains in one state all the time.

In the on-site application the CRT internal oscillator is switched off, a coherent signal from the radar is applied to the external input, and the output of the CRT is connected to the radar front end test point input. Except for RF switch A8, the CRT functions the same as in the remote application. Switch A8 and the 180° hybrid (A7) provide a doppler shift calibration for coherent radars, alternately switching between the 0° line and the 180° line every radar pulse.

The CRT is expected to operate normally over an ambient temperature range of -30°C to +50°C. A thermostatically-controlled fan is switched on at the high temperature range, and provision for a heater has been included for operation at the low temperature range. The enclosure can be sealed (if additional air ducting is included) and exposed to outside weather with only the input/output coaxial connector and the AC power cord accessible. Normal operation is with the top half of the enclosure removed allowing access to the control panel and test points.

SECTION 3. INSTALLATION AND OPERATION

3.1 Input/Output Characteristics

It is absolutely necessary that the peak power level of the radar pulse to be applied to J1 be known! The reference level of the detector (A19) is approximately 0 dBm; burn-out level is approximately +20 dBm. The appropriate attenuator (A17) must be inserted before the radar pulse is applied to J1.

Table 3-1 lists the input/output characteristics of the CRT.

TABLE 3-1. INPUT/OUTPUT CHARACTERISTICS

Connector	Characteristics
AC Power	• 115 VAC, 60 Hz, approximately 120 watts w/o heater.
J1	• 50 Ω, type 'N' Jack.
Input Signal	• maximum of 400 watts peak with all attenuators (A17) inserted. • 2700 - 2900 MHz
Output Signal	• 0 dBm, internal source • 18 dB below external source input
J2 Enable Input	• High impedance, BNC Jack • Open, or TTL "high", enables CRT • TTL "low" disables CRT
J3 External Source	• 50 Ω, type 'N' Jack +20 dBm maximum input

3.2 Installation Procedure

The following procedure should be followed at the time of installation:

CAUTION

Peak power at detector input greater than +20 dBm will destroy the detector diode.

---

1. Insert appropriate attenuator values (A17) between the coupler (A16) and variable attenuator (A18) to reduce the radar signal level at the input of the variable attenuator to between 0 dBm and +10 dBm.

2. Adjust the variable attenuator (A18) for maximum attenuation (fully CCW).

3. Apply power to the CRT and place MODE switch to TEST.

4. Apply the radar signal to J1.

5. Reduce attenuation (A18 - adj. CW) until the REFERENCE LEVEL light just comes on (the LED will flicker, depending upon the PRF of the radar). This establishes the reference level midway between comparators 13 and 14, and produces a 1 1 1 0 0 code. A decrease of 1/2 dB in the radar input power level will change the code to 1 1 0 1 1; an increase of 1/2 dB will change the code to 1 1 1 0 1.

3.3 Operation

The response times of the coded signal are determined by the settings of the three sets of thumb switches on the control panel (see response timing, Figure 2-2). These switches provide delays in multiples of 10 μsec. A ten-turn potentiometer (U67) on the Timing and Control card (A2) provides an additional continuously variable 2 to 10 μsec delay in the T1 start time. A summary of all the controls for the CRT is given in Table 3-2.

TABLE 3-2. CRT CONTROLS

Control Panel

POWER	ON/OFF	
MODE	OPERATE	Normal operation.
	TEST	For installation and test. • Reference Level indicator is enabled. • RF switch A10 directs RF signal to termination AT-2.
SOURCE	INTERNAL	• RF oscillator A5 is activated. • RF switch A8 is held in one state (no phase shift).
	EXTERNAL	• RF oscillator A5 is deactivated • RF switch A8 is activated
RESPONSE TIME	T1, T2, T3 0-99	Selects delay in multiples of 10 μsec

Internal

Attenuator A18		Provides up to approximately 15 dB variable attenuation.
A2, Potentiometer U67		Provides continuously variable delay of 2 to 10 μsec for T1.
A2, Switch U56		
SW-1	ON	Response pulse width is 2 μs for T1, T2, T3.
	OFF	Response pulse width is 2 μs for T1, 4 μs for T2, and 8 μs for T3.
SW-2	ON	Response amplitude alternates 20 dB every 1024 radar pulses.
	OFF	Response amplitude alternates 20 dB every 2048 radar pulses.
SW-3	ON	Normal operation - RF switch A10 controlled by coding and by OPERATE/TEST control.
	OFF	RF switch A10 in one state such that a CW signal is produced at J1.
SW-4	ON	RF switch A8 held in one state, resulting in no phase shift.
	OFF	Normal operation - RF switch A8 alternates when CRT is in External Source mode.

SECTION 4. DETAILED DESCRIPTION

4.1 Timing and Control Card (A2)

4.1.1 Reset and Start

A block diagram of the reset and start circuitry is given in Figure 4-1 and the corresponding timing sequence is given in Figure 4-2. The start pulse is applied to two one-shot (o.s.) multivibrators, one which produces a 1 μs wide pulse and another which produces a variable (0.2 to 0.4 μs) width pulse. The 1 μs pulse provides a delay before starting the clock while the variable pulse resets all the digital functions. This reset pulse is variable because it also starts the HOLD time for the sample-and-hold on the A/D converter card and therefore allows for optimization of this function.

The reset pulse also starts a 2 μs one-shot pulse, at the end of which a 0.2 μs LOAD pulse is generated. The combined time of these two pulses determines the duration of the HOLD pulse. The LOAD pulse is used elsewhere on the card to load data into a shift register.

Up to this point everything depends upon just the start pulse (with ENABLE high). Now a check is made to see if the radar pulse amplitude is large enough (greater than -12 dB reference) to warrant a response. The load pulse clocks a register and if the first comparator of the A/D card has been activated, the remaining operations continue. The 1024/2048 counter is advanced by one and when the count of either 1024 or 2048 (determined by SW-2) is reached, a flip-flop is activated which changes the state of RF switches A11 and A12 (for the 20 dB response step). A flip-flop which changes the state of RF switch A8 (phase shift) is also activated if not inhibited by SW-4 or by internal mode operation. If the first comparator has not been activated ($\overline{\text{COMP-1}}$ is low), the clock enable is reset, stopping the clock and the RF switch logic is not activated.

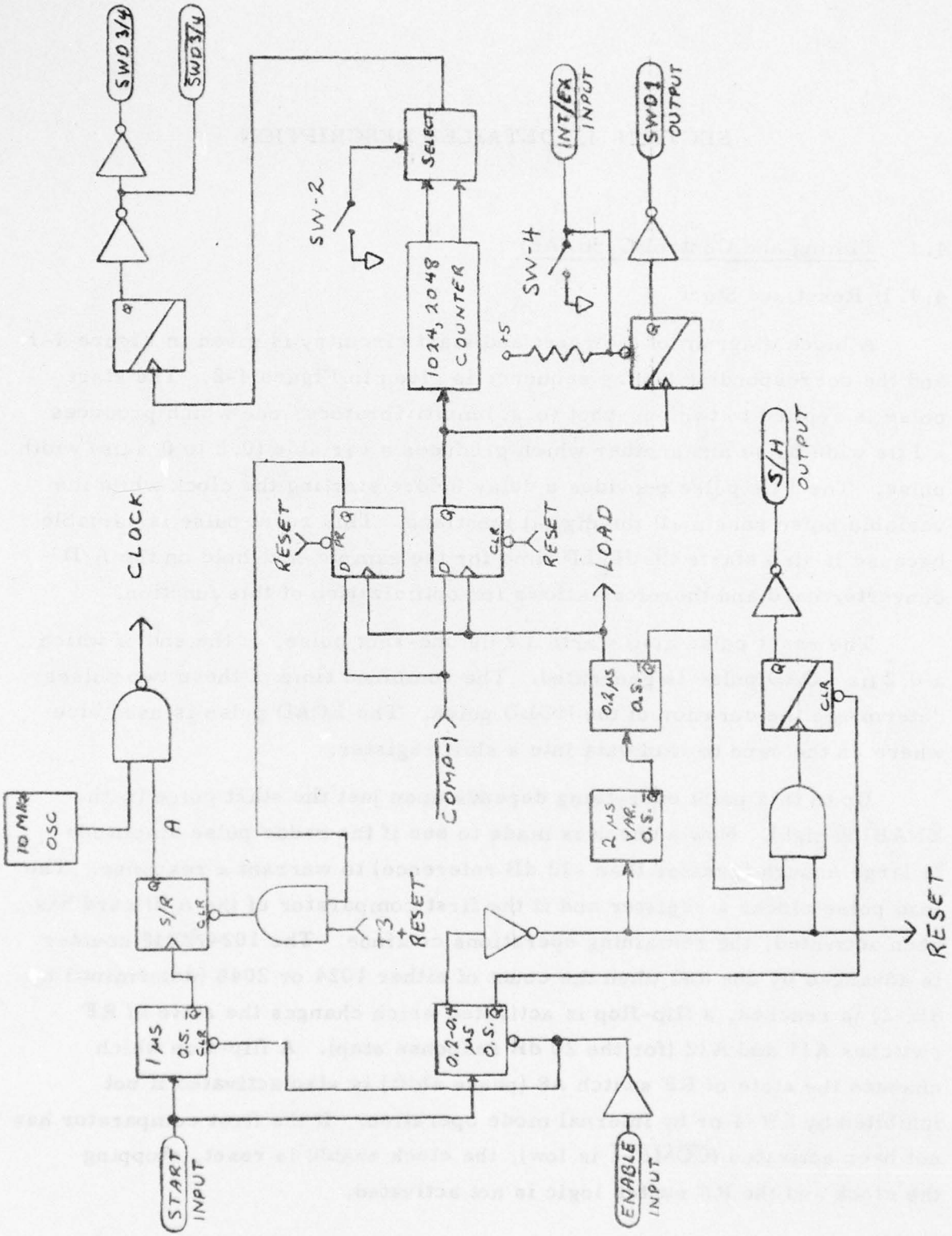


Figure 4-1. Timing and Control Reset and Start Block Diagram

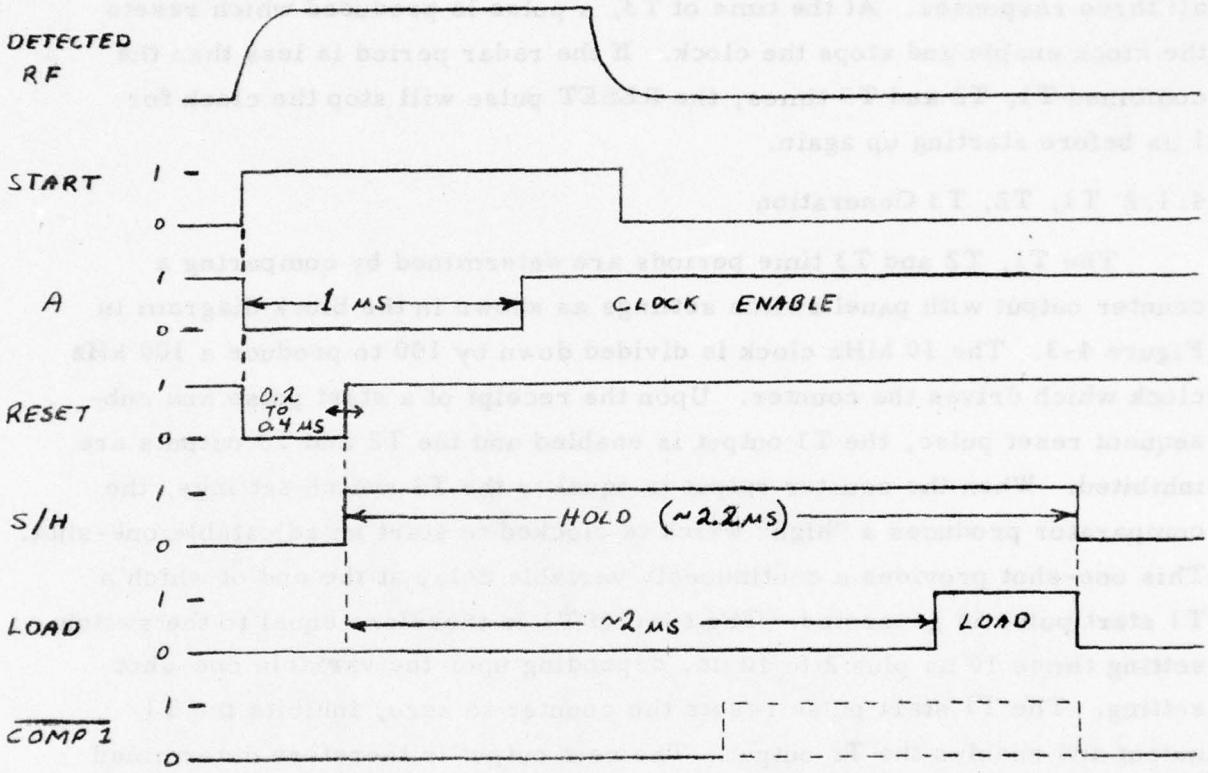


Figure 4-2. Reset and Start Timing

The clock will be stopped by two other conditions, in addition to the one just mentioned. If the T1, T2 and T3 settings are such that their combined time is less than the radar period, the transponder will produce all three responses. At the time of T3, a pulse is produced which resets the clock enable and stops the clock. If the radar period is less than the combined T1, T2 and T3 times, the RESET pulse will stop the clock for 1 μs before starting up again.

4.1.2 T1, T2, T3 Generation

The T1, T2 and T3 time periods are determined by comparing a counter output with panel switch settings as shown in the block diagram in Figure 4-3. The 10 MHz clock is divided down by 100 to produce a 100 kHz clock which drives the counter. Upon the receipt of a start pulse and subsequent reset pulse, the T1 output is enabled and the T2 and T3 outputs are inhibited. When the counter output is equal to the T1 switch settings, the comparator produces a "high" which is clocked to start an adjustable one-shot. This one-shot provides a continuously variable delay at the end of which a T1 start pulse is generated. The time of T1 is therefore equal to the switch setting times 10 μs plus 2 to 10 μs, depending upon the variable one-shot setting. The T1 start pulse resets the counter to zero, inhibits the T1 output and enables the T2 output. The next output is therefore determined by the T2 switch setting. Likewise, the T2 start pulse resets the counter, inhibits the T2 output and enables the T3 output. The T3 start pulse inhibits the T3 output and stops the clock. T2 and T3 have no variable adjustment and are therefore integral multiples of 10 μs.

4.1.3 Serial Code Generation

The 16 lines from the comparators are encoded into a four-bit word which along with the reference bit ($\overline{\text{COMP-1}}$) is loaded into the parallel-to-serial shift register. The shift register is ten bits long and the 5 data bits are loaded into the even numbered cells. The odd numbered cells are loaded with hard-wired "zeros" (Figure 4-4).

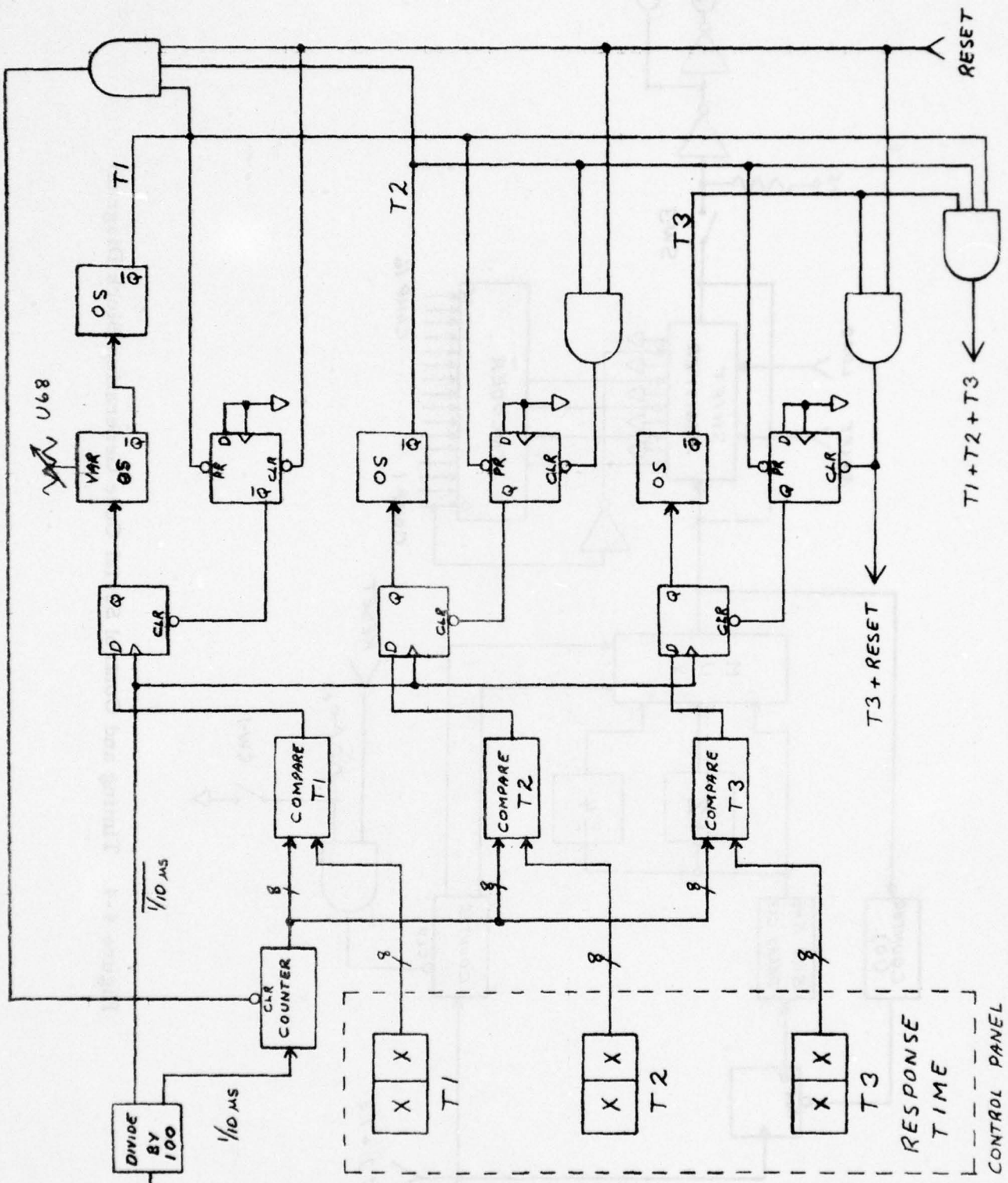


Figure 4-3. Timing and Control T1, T2, T3 Generation Block Diagram

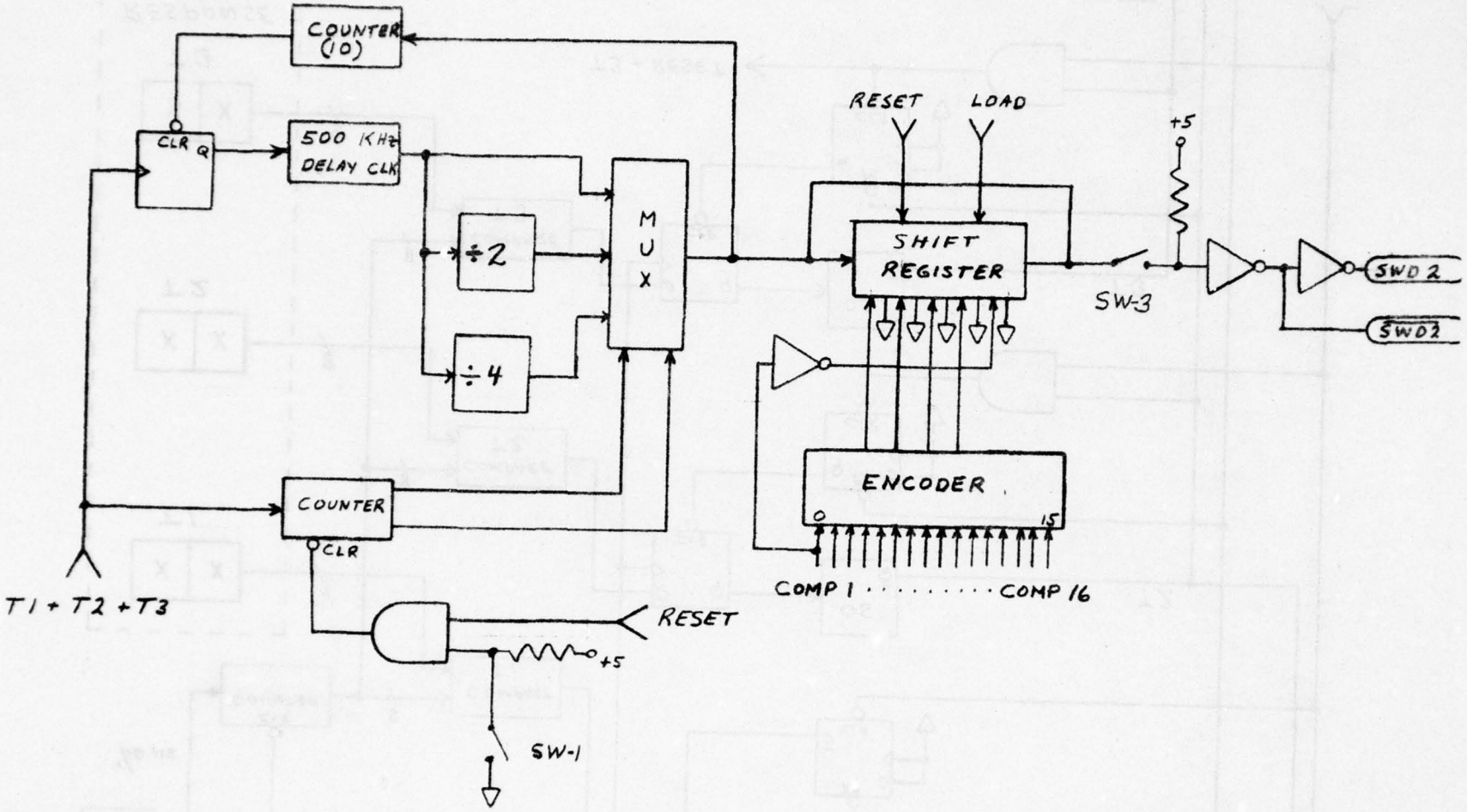


Figure 4-4. Timing and Control Serial Code Generation Block Diagram

The T1 start pulse starts a 500 kHz clock which is applied to the shift register through a multiplexer. A counter allows exactly ten clock pulses to trigger the shift register which therefore cycles its data once. The 500 kHz clock is divided by two and by four and each of the resultant clocks is applied to a multiplexer input. Switch SW-1 controls another counter which addresses the multiplexer and selects one of the three clock inputs to be applied to the shift register. In one switch position the same 500 kHz clock is used for each of the T1, T2 and T3 responses. The resultant RF code is the same for each group of responses; 2.0 μs pulse width. With the switch in the other position, a different clock is selected for each pulse group: T1 has a 2.0 μs pulse width, T2 a 4.0 μs pulse width and T3 an 8.0 μs pulse width.

The buffered shift register output drives the switch drivers for RF switch A10 which gates the microwave signal to produce the coded response. Switch SW-3 disconnects the code generator from the switch drivers and causes them to produce a CW response at the CRT output (J1).

4.2 A/D Converter Card (A3)

The A/D Converter card contains a video amplifier, a sample-and-hold circuit and a bank of voltage comparators as shown in Figure 4-5.

The detected RF pulse is inverted, amplified by a factor of about 10, and applied to the FET switch of the S/H circuit and to a fast comparator. This comparator has a low threshold level and generates the start pulse which triggers the Timing and Control card. The Timing and Control card generates the S/H waveform (see Figure 4-2) as described in section 4.1.1. The S/H pulse causes the FET switch to open and the R-C network "stores" the detected pulse amplitude while each of the remaining comparators "compares" this value with its respective preset reference level. These reference levels are adjustable and are set to match the RF detector characteristics to provide the 1 dB steps in amplitude measurement.

In addition to the start comparator and the sixteen level comparators, a separate comparator is used to indicate the RF input reference amplitude during installation or test. This comparator has a reference level set

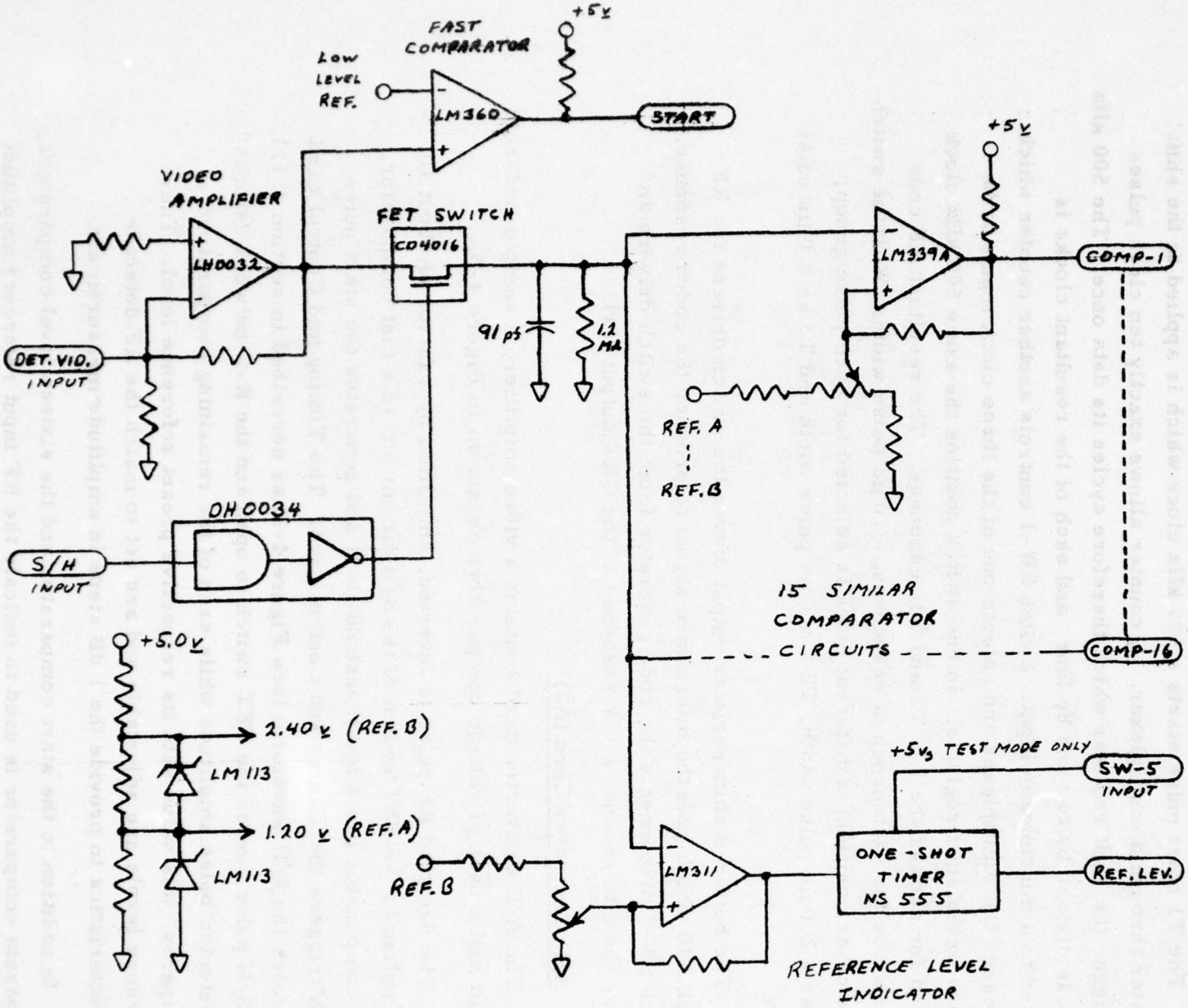


Figure 4-5. Functional Diagram of the A/D Converter Card

midway between those of comparators 13 and 14. During test mode operation when the video pulse exceeds this level, the comparator triggers a one-shot pulse generator (~1 ms pulse width) which lights a control panel LED.

4.3 Switch Driver Card (A4)

The Switch Driver card contains the drivers for all the RF switches plus the temperature sensing circuitry for the fan and heater (if implemented).

There are two types of driver circuits used as shown in Figure 4-6. RF switch A10 produces the coded response pulses and must change states moderately fast (~ 0.1 μsec). This requires a driver which produces current spikes at the transition times. The remaining RF switches (A8, A10 and A11) have moderate switching speed requirements (few μsec) and do not need the current spikes.

The temperature sensing circuitry consists of two voltage comparators and a balanced bridge with a negative-coefficient thermistor (located elsewhere) in one arm. When the ambient temperature is above a preset level, one comparator will activate a relay which turns on the fan. When the temperature is below another lower preset level, the other comparator activates another relay which applies power to the heaters (if installed). Hysteresis is used in the comparator designs to prevent on-off oscillations.

4.4 Microwave Circuitry

The signal received by the CRT horn antenna (16 dB gain) can range in power level from 10 to 400 watts peak, depending upon the installation site (see Appendix A). The input circulator (A15-Figure 2-1) is capable of handling this peak power, but other components in the CRT will be damaged or destroyed by power levels greater than one watt, and the RF detector (A19) will be destroyed by an incident power level greater than 100 milliwatts.

A total attenuation value of up to 56 dB is needed to reduce the radar signal power at J1 to the operating level of the detector. This is accomplished by the 20 dB coupler (A16), 10 dB and 20 dB fixed pads (A17), and the variable attenuator (A18). Separate 10 dB and 20 dB pads, inserted as necessary, are used rather than a 0 to 40 dB variable attenuator because

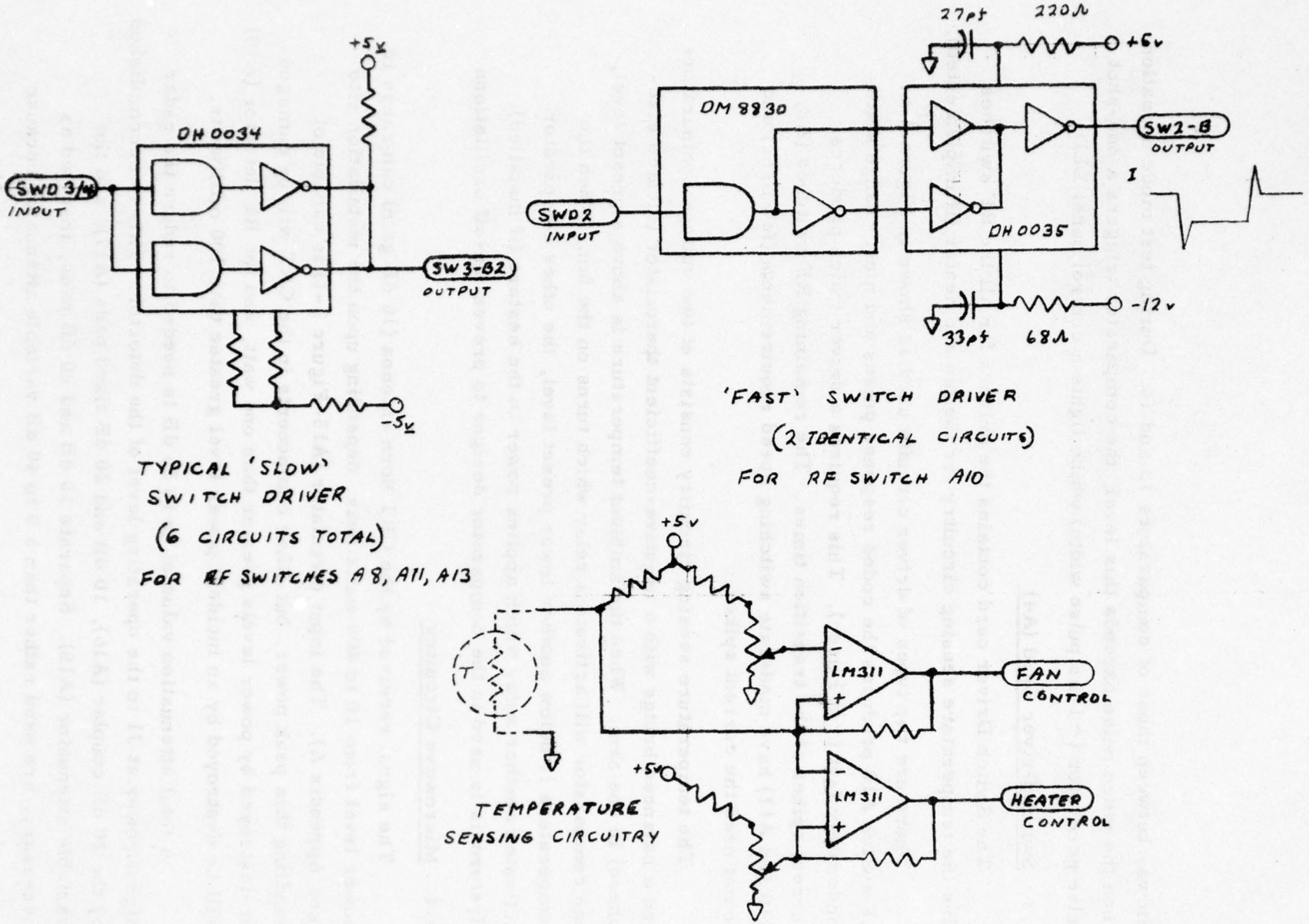


Figure 4-6. Functional Diagram of the Switch Driver Card

the latter has a large temperature coefficient. Minimum amplitude variation over temperature is therefore achieved by using as little attenuation in the variable attenuator as possible and removing or inserting the fixed pads as required.

The RF detector (A19) uses a tunnel diode which has excellent temperature stability compared to the Schottky diode and crystal detectors. The normal operating point (0 dB reference level) of the detector is minus 2 dBm, at which level it produces approximately 150 mV into a 180 ohm load (video amplifier of A3).

The input circulator provides approximately 20 dB of isolation between the input port (#1) the third port (#3). This means that with peak input powers greater than 100 watts, leakage power at port #3 can be greater than 1 watt, the peak power limitation of the solid-state RF switches. A limiter (A14) is therefore included to protect the switches from this excessive power. It passes almost unattenuated a signal of peak power less than 5 mW, but reflects signals greater than that. Its maximum leakage power is no greater than 150 mW, well below the maximum power limitation of the switch.

The internal RF source (A5) is a tunable phase-locked cavity oscillator (PLO) with a replaceable reference crystal. Frequency stability requirements over temperature and time (one month) dictates the use of a crystal source, while system versatility requires a tunable source for different installations. This phase-locked oscillator meets both these requirements by using field replaceable crystals. Complete crystal replacement and tune up procedures are given in Appendix B. With no crystal installed, the PLO can be used as a standard cavity-tuned source by disabling an internal sweep circuit.

A circulator (A6) is placed on the output of the oscillator to prevent pulling of the frequency by RF load changes. Slow, gradual load changes are compensated for by the phase-locking feature, but fast abrupt load changes (such as from switching transients) can cause the oscillator to lose

lock momentarily. Even though an internal sweep mechanism will cause it to reacquire, this interruption of response is unacceptable if frequently occurring. The circulator greatly reduces the chance of this happening.

The 180° hybrid (A7) and the SPDT switch (A8) combination produce a one-bit phase shift when used with an external source. A signal fed into the Δ arm of the hybrid is split into two equal amplitude signals differing in phase by 180°. The RF switch alternately selects the 0° phase and 180° phase signals every radar pulse. Switch A8 is a non-reflective switch which means that both outputs of the hybrid "see" a good match no matter which state the switch is in, thus insuring proper balance of the hybrid. A signal fed into the Σ arm of the hybrid is also split into two equal amplitude signals, but in this case they are also of equal phase.

The remaining RF switches (A10, A11, A12) are standard reflective type switches. Switch A10 produces the pulse-coded response signal by switching the source signal from the termination to the output circuitry. Switches A11 and A12 operate simultaneously and essentially insert either a no loss line or a 20 dB attenuator (A13) into the response signal path.

APPENDIX A

INSTALLATION SITE CONSIDERATIONS

The pertinent characteristics of the three known installation sites are given in Table A-1. It can be seen from this data that the CRT has ample transmission power capability, and in fact may have too much for the Spandar installation. Additional attenuation can easily be inserted between J1 and the horn antenna if necessary.

The Spandar site presently has a tower and horn installation which has been used successfully. For the remaining two sites careful consideration should be given to the exact location of the CRT horn antenna to avoid the typical low-angle radar problems such as ground reflections. It should also be noted that the CRT horn has a fairly wide beamwidth (~28°) and no frequency filtering (other than typical waveguide or octave bandwidth components) and is therefore susceptible to being triggered by other radars in the area.

TABLE A-1. INSTALLATION SITES

Radar Site	Spandar	Cimmaron	Sudbury
Frequency	2840.0 MHz	2735.0 MHz	~2800 MHz
Power	4 mW	0.5 mW	1.0 mW
Antenna Gain	50.6 dB	46 dB	~46 dB
Pulse Width	1, 2 μs	1 μs	~1 μs
IF BW	?	0.65 MHz	?
Receiver Dyn. Range	-40 dBm max.	-30 → -110 dBm	?
CRT Installation Range	3.1 km	~2.5 km	6.6 km
Power Received at CRT Horn	400 W (+ 56 dBm)	50 W (+47 dBm)	10 W (+40 dBm)
CRT Power Received by radar antenna (0 dBm transmitted)	-40 dBm (-45 dBm with one-way cable loss of 5 dB)	-40 dBm	-51 dBm
Return Power from Weather at 100 km for: 40 dBz	-51 dBm	-64 dBm	-61 dBm
20 dBz	-71 dBm	-84 dBm	-81 dBm
0 dBz	-91 dBm	-104 dBm	-101 dBm

APPENDIX B

PHASE-LOCKED OSCILLATOR CRYSTAL REPLACEMENT AND TUNE-UP PROCEDURE

The following three (3) pages contain the manufacturer's crystal replacement and tune-up procedures for the phase-locked oscillator. Inapplicable sections have been cross-hatched off.

This oscillator uses a multiplication factor of 27 for the reference. Therefore, the required crystal frequency is determined by dividing the desired output frequency by 27. For example, the delivered unit has an output frequency of 2840.0 MHz and the crystal frequency is 105.1852 MHz. Crystals used should meet Frequency West Specification 37-051991 (suggested vendor is Croven-Canada).

FREQUENCY-WEST, INC.

TUNEUP PROCEDURE – PHASE-LOCKED SOURCES AND OSCILLATORS

INTRODUCTION

■■ These instructions cover the crystal installation and alignment procedures for Frequency West crystal controlled phase locked sources and oscillators. The procedures cover the various equipment models and are organized by sections listed below. The user should perform only those procedural steps that apply to his own equipment.

Section	Equipment
Crystal Installation	
Sources without Ovens	Equipment model numbers ending in: X, XA, XB
Sources with Ovens	Equipment model numbers ending in: XO and XC
Alignment Procedures	
Preliminary Setup – Sources Using External Reference Oscillator	Equipment model numbers ending in: XE
Alignment – All Phase Locked Sources and Oscillators	All equipment

*NOTE: Supplied PLO has slightly different mechanical configuration.

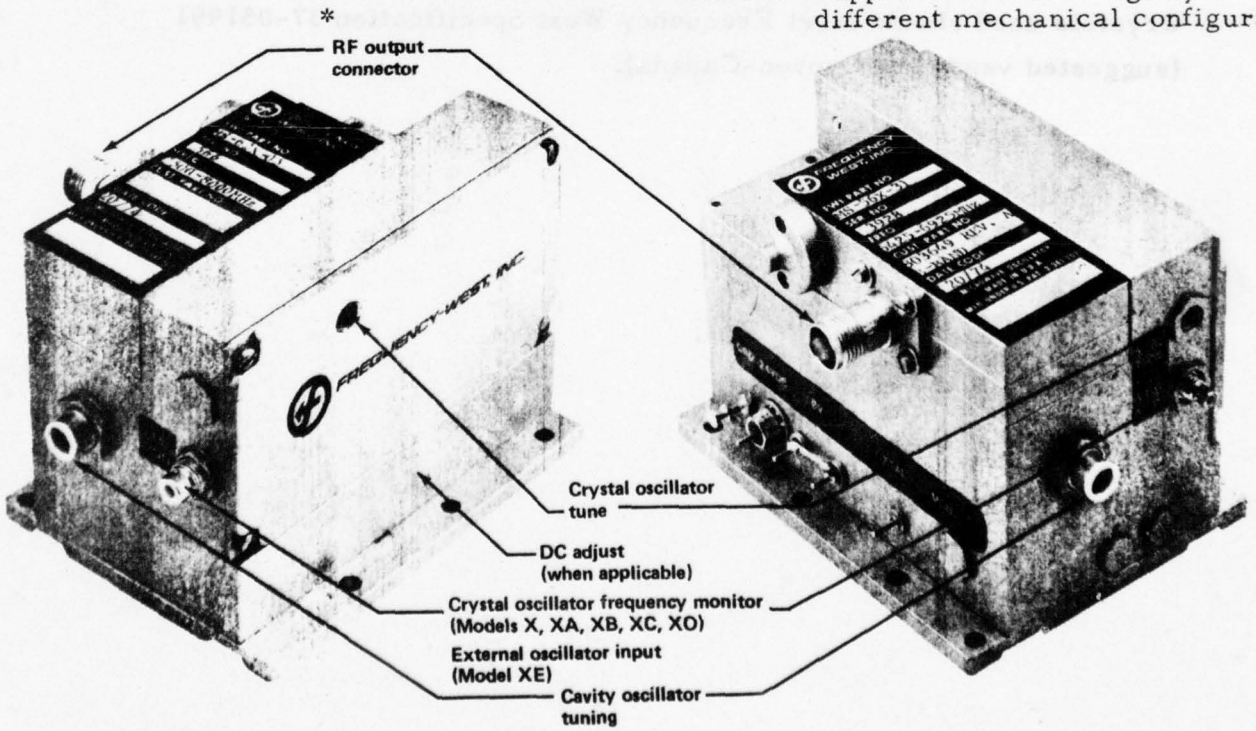


Figure 1

CRYSTAL INSTALLATION

- **Sources without Ovens**

1. Remove the side plate bearing the Frequency West logo from the unit (held by four screws).

2. Clip the replacement crystal leads to between 0.150 and 0.190 inch in length. Insert the crystal in its socket. See Figure 2. For best results use crystals meeting Frequency West Specifications 37-051990 and 37-051991.

3. Replace the side plate.

4. Proceed to *Alignment – All Phase Locked Sources and Oscillators.*

- **Sources with Ovens**

1. Remove the side plate bearing the Frequency West logo from the unit, the oven insulator, crystal heat sink, and the crystal. See Figure 3.

2. Clip the replacement crystal leads to between 0.150 and 0.190 inch in length. Insert the crystal into its socket. For best results use crystals meeting Frequency West Specification 37-052243.

3. Replace the crystal heat sink, insuring that the heat sink slot clears the oven thermistor wire. Replace the oven insulator and side plate.

4. Proceed to *Alignment – All Phase Locked Sources and Oscillators.*

ALIGNMENT PROCEDURES

- **Preliminary Setup – Sources Using External Reference Oscillator**

1. Turn the fundamental oscillator tuning screw counterclockwise until the source is tuned to the lowest frequency of the operating band while monitoring the source frequency with a frequency meter or counter.

2. Divide the desired output frequency by the net multiplier ratio (see Table 1 or 2) to obtain the required reference input frequency from the external crystal oscillator or frequency synthesizer.

3. Connect the external oscillator to the source reference oscillator input jack. (Input power requirement is 0 to +10 dBm; 50 ohms nominal impedance.)

4. Proceed to *Alignment – All Phase Locked Sources and Oscillators.*

- **Alignment – All Phase Locked Sources and Oscillators**

1. Apply the specified input (supply) voltage between the DC input terminal and ground. The required input voltage is indicated above the terminal.

NOTE

Sources with odd model numbers require positive power supply input voltages; those with even model numbers require negative input voltages. The procedure below applies to both types of units; however, the polarity of the voltages listed in the various steps must be reversed for those sources with positive voltage power supplies.

2. Connect a VOM to the crystal oscillator test point (XTAL). Set the VOM on the +1.5 VDC scale. The typical voltage level at this point will be 0.2 volts.

NOTE

Step 3 does not apply to units using external reference oscillators.

3. Tune the crystal oscillator coil, or capacitor (through a hole in the side plate or the front plate, depending on the configuration) until a reading is obtained (approximately 0.2V). Maximize this reading.

A maximized VOM reading at this point can be expected to yield a crystal oscillator accuracy within approximately 5 ppm of the marked crystal frequency.

If a frequency counter is available, connect the counter to the crystal oscillator monitor connector and tune the crystal oscillator to the exact frequency. Make sure that the crystal oscillator is not near dropout by rocking the tuning screw back and forth. The unit should tune a minimum of 5 ppm, or 500 Hz at 100 MHz.

Reset the crystal frequency to the correct frequency.

4. Connect an oscilloscope or VOM to one of the phase voltage terminals (ϕ V). The two terminals should be jumpered together on units with two terminals. For sources that have a lock limit alarm, connect the scope or VOM to the single phase voltage terminal. The scope should show a waveform of between 50 and 500 Hz, with an amplitude greater than 12V p-p. The VOM should read approximately 9 volts on the AC (rms) scale.

5. If no AC waveform appears, adjust the DC balance potentiometer (under the crystal side plate) until the waveform appears. (Most units manufactured after August, 1973 do not require this adjustment.)

Find the middle of this adjustment, or adjust the potentiometer for either the highest frequency waveform (triangular or square wave, depending on the source model) or for the highest reading on the AC VOM.

6. Slowly tune the fundamental oscillator tuning screw clockwise until the waveform drops out or the AC voltage drops to zero on the VOM.

If the unit has a crystal that places the output frequency at the high end of the band, it may be necessary to continue to tune until a second lock occurs. Check for the proper lock point with a frequency meter or counter to insure locking on the correct harmonic of the reference oscillator.

7. Switch the scope to DC (2 V/cm scale) or the VOM to 30 VDC full scale. (The leads should still be connected between the phase lock terminal and ground.)

8. Check for lock by rocking the fundamental oscillator tuning screw slightly. The absolute magnitude should decrease as the tuning screw is rotated clockwise.

If the voltage does not change, the unit has not locked and has stopped sweeping. Repeat steps 4 and 5, then continue tuning the fundamental oscillator until lock occurs.

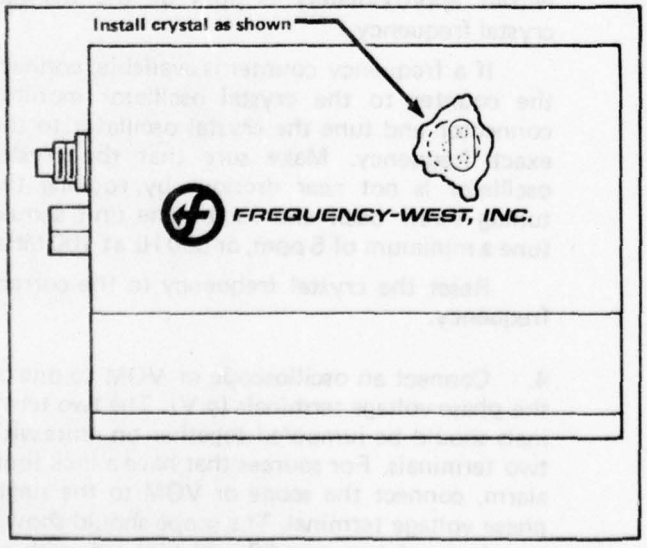


Figure 2

9. Tune the fundamental oscillator to the edge of the phase lock range. This should be between −3V ±2V and −16V ±2V. The unit should remain locked between these voltages and go into sweep as the fundamental oscillator is tuned further. This verifies that the unit remains phase locked over the appropriate tuning voltage range.

10. Set the fundamental oscillator so that the voltage at the phase lock terminals is −7.5 volts. Tuneup is complete.

NOTE

For units with lock limit alarm: To verify the operation of the lock limit alarm circuitry, connect a VOM (x10 ohm scale) between the lock limit terminal and ground. As the unit is tuned from one end of the lock range to the other (−3V ±2V to −16V ±2V), the VOM will read either zero or infinity. It will be infinity between approximately 4.5 and 13VDC (as read at the phase lock terminals), and zero elsewhere.

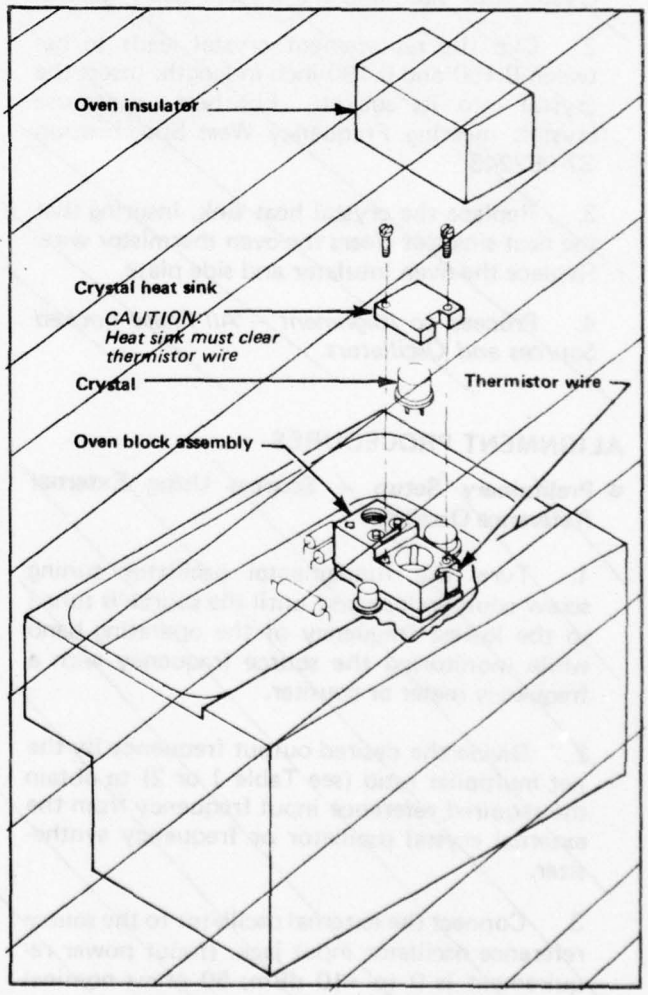


Figure 3

APPENDIX C

PRODUCT INFORMATION

1. Phase-Locked Oscillator (A5)

Manufacturer	Frequency-West, Inc., Santa Clara, CA
Model Number	MO-118-XB
Min. Power Output	20 mW
Mech. Tunable Frequency Rnage	2.70 - 3.22 GHz
Operating Temperature	-30°C to +60°C
Frequency Stability	Crystal, ± 0.002%
Spurious, Harmonics	60 dB below carrier (in-band) 20 dB below carrier (out-of-band)
Input Power	-20 VDC ± 1.5%

2. *Circulators (A6, A15)*

Manufacturer	P & H Laboratories, Chatsworth, CA
Model Number	B1-S35310
Frequency	2.7 - 2.9 GHz (optimized)
Insertion Loss	0.3 dB typ.
VSWR	1.2:1 max.
Isolation	20 dB min
Power Handling Capability	50 Watts avg., 1 kW peak

3. 180° Hybrid (A7)

Manufacturer	Anaren Microwave, Syracuse, N.Y.
Model Number	30056
Frequency	2-4 GHz
Insertion Loss	0.5 dB max.
VSWR	1.3:1 max.
Isolation	15/18 dB min./typ.
Amplitude Balance	± 0.50 dB
Phase Balance	± 6 deg.

4. Single-Pole Double-Throw Switch (A8) - (Non-reflective)

Manufacturer	Alpha Industries, Woburn, MA
Model Number	MT-3685-A-P3-Q1
Frequency	0.5 - 4 GHz
Insertion Loss	1.1 dB max.
VSWR	1.5:1 max.
Isolation	50 dB min.
Power Handling Capability	1 Watt CW

5. Fixed Attenuators (A9, A13, A17, A22)

Manufacturer	Narda Microwave, Plainview, NY
Model Number	4772-(Value)
Frequency	DC-6 GHz
VSWR	1.25:1 (to 4 GHz) max.
Attenuation Accuracy	$\pm$ 0.3 dB
Power Handling Capability	2 Watts avg., 0.2 kW peak

6. Single-Pole Double-Throw Switch (A10)

Manufacturer	Alpha Industries, Woburn, MA
Model Number	MT-3121A4
Frequency	2-4 GHz
Insertion Loss	0.9 dB max.
VSWR	1.5:1 max.
Isolation	60 dB min.
Switching Speed	20 ns typ.
Power Handling Capability	1 Watt CW

7. Single-Pole Double-Throw Switches (A11, A12)

Manufacturer	Alpha Industries, Woburn, MA
Model Number	MT-3127A4
Frequency	2-4 GHz
Insertion Loss	0.8 dB max.
VSWR	1.5:1 max.
Isolation	60 dB min.
Power Handling Capability	1 Watt CW

8. Limiter (A14)

Manufacturer	Alpha-Industries, Woburn, MA
Model Number	MT-3260A4
Frequency	2-4 GHz
Insertion Loss (-10 dBm input)	0.6 dB max.
VSWR (-10 dBm input)	1.4:1 max.
Limiting Threshold (input)	5 mW
Leakage Power	
1 Watt CW input	65 mW
200 Watt peak input (1 μs)	150 mW

9. Coupler, 20 dB (A16)

Manufacturer	Narda Microwave, Plainview, NY
Model Number	4013C-20
Frequency	2-4 GHz
Insertion Loss	0.2 dB max.
VSWR	1.15:1 max.
Directivity	22 dB min.
Power Handling Capability	50 Watts avg., 3 kW peak

10. Variable Attenuator (A18)

Manufacturer	Merrimac Industries, West Caldwell, NJ
Model Number	AUM-15A
Frequency	2-8 GHz
VSWR	1.5:1 max.
Attenuation Range (2 GHz)	0.5 to 15 dB
Power Handling Capability	2 Watts avg.

11. RF Detector (A19)

Manufacturer	Microwave Associates, Burlington, MA
Model Number	MA 7700K-M07
Frequency	2-4 GHz
VSWR	2:1
Detection Sensitivity	700 mV/mW (-20 dBm, open circuit)
Power Handling Capability	~20 dBm (100 mW) max.

12. Power Supply, 20V (A20)

Manufacturer	Sorensen, Manchester, NH
Model Number	QSA 18-1.9
Output Voltage	14-22 VDC
Output Current (50°C)	0 - 1.9 ADC
Constant Voltage Regulation	± 0.005%
Constant Voltage Ripple	300 μV rms

13. Power Supply, 5V (A21)

Manufacturer	Sorensen, Manchester, NH
Model Number	QSA 10 - 3.7
Output Voltage	0 - 10 VDC
Output Current	0 - 3.7 ADC
Constant Voltage Regulation	± 0.005%
Constant Voltage Ripple	300 μV rms

14. Additional Main Assembly (A1) Parts List

Designation	Description	Manufacturer & Model Number
AT1, 2, 3	Terminations	Narda 4370 DM
CP1, 2, 3	SMA Male-Male Adapter	OSM 218-07
Q1	-5V Regulator	LM 320K-05
Q2	-12V Regulator	LM 320K-12
K1, K2	Hybrid Relay	Magnecraft W501QPCX-11
Z1	Thermistor	Fenwal GB41J1
F1	Fan	Rotron MU2A1
S4-S9	BCD Switch	Digitran 8011

15. Timing and Control Card (A2) Major Parts List

Designation	Description
U1, 12	SN7406 (2)
U2, 3	SN74148 (2)
U4, 40	SN7404 (2)
U5, 6, 7, 17, 18, 19	SN7485 (6)
U8, 20, 32, 44, 51	SN74160 (5)
U10, 25, 35, 38, 42, 43	SN74123 (6)
U14, 15	SN7496 (2)
U16, 34	SN7400 (2)
U22, 53	SN7408 (2)
U23, 24, 27, 28, 29, 30, 31, 39, 58, 59	SN7474 (10)
U26	SN74153 (1)
U33	SN7414 (1)
U36, 48, 60	SN74161 (3)
U41	SN7410 (1)
U46	SN7437 (1)
U21, 52 (Resistor Network)	Sprague 916C102X5PD (2)
U45 (Oscillator)	Greenray ZY-7409 (1)
U56 (Switch)	AMP 435166-2 (1)

16. A/D Converter Card (A3) Major Parts List

Designation	Description
U1	LH0032CG
U2	CD4016AE
U3	DH0034CD
U4 (Resistor Network)	916C472X5PE
U5	LM555CN
U6	LM311N
U7-U10	LM339AD
U11	LM360H
U12, U13	LM113H

17. Switch Driver Card (A4) Major Parts List

Designation	Description
U1, U2	DH0035CG
U3	DM8830N
U4-U9	DH0034CD
U10, U11	LM311N
D1, D2	1N752A

APPENDIX D

DRAWINGS FOR THE CRT

Size	Title (Electrical)	Drawing Number
D	Interconnection Diagram (A1)	SD 975605
D	Timing and Control Card (A2)	SD 975604
C	A/D Converter Schematic Diagram (A3)	SD 975603
C	Switch Driver Schematic Diagram (A4)	SD 975602

	Title (Mechanical)	
A	Spacer	975593
B	RF Bracket	975596
B	Conn Bracket	975597
B	PCB Support Bracket	975595
C	Corner Brackets	975600
C	Control Panel	975601
B	Mounting Brackets	975594
C	P.S. Plate	975598
C	Upper Level Bracket	975599

TABLE OF CONTENTS
VOLUME II

LIST OF ILLUSTRATIONS

SECTION 1. INTRODUCTION

The Pulse Pair Processor (PPP) is a digital real-time signal processor designed by Raytheon for AFGL under contract No. F19628-72-C-0293 and described in the associated Equipment Information Report. The PPP computes first and second spectral moments of returns from any coherent meteorological radar for each of more than 1000 range cells of 0.5, 1, or 2 microseconds duration.

The Ground Clutter Canceller, described in this Equipment Information Report, was designed, constructed and installed in the PPP under contract F19628-76-C-0297. The canceller is a digital filter designed to reject unwanted ground clutter and coherent oscillator feed-through, thereby improving the sensitivity and accuracy of spectrum mean and width estimates.

SECTION 2. GENERAL DESCRIPTION

The synthesis of a digital filter for incorporation into the Pulse Pair Processor (PPP) for the purpose of rejecting unwanted ground-clutter interference has been described in Reference 1. This section describes the hardware design of the filter in general terms and indicates how the individual modules are interconnected and interfaced with the modified PPP. The circuit design of each module is discussed in detail in SECTION 4.

The approach which has been adopted for this implementation to meet the requirements listed in Table 2-1 begins with a design of the simplest possible digital filter module which meets the dynamic range and accuracy requirements by taking advantage of the economies possible with low-power Schottky serial two's-complement arithmetic elements (Reference 2) and NMOS random-access memories. The inadequate throughput rate of the resulting module is then overcome by multiplexing as many of the modules as required, with each of them assigned to range cells adequately spaced in time to match its throughput. The resulting filter is one where both memory and arithmetic processing elements are distributed rather than centralized as in the traditional general purpose computer architecture. While the basic form of the filter is "hard wired" within each module, some flexibility is achieved by distributing gain constants and timing signals from a single programmable read-only memory via busses to all of the modules. The eight-module version attains an impressive processing rate of 16 multiplications (16 x 16), 24 additions, and 24 memory references per microsecond.

References: 1. H. L. Groginsky memo HLG-365, "Weather Radar Canceller Design", dated 17 May 1976.

2. "Digital Signal Processing Handbook", John R. Mick, Advanced Micro Devices, Inc. 1976.

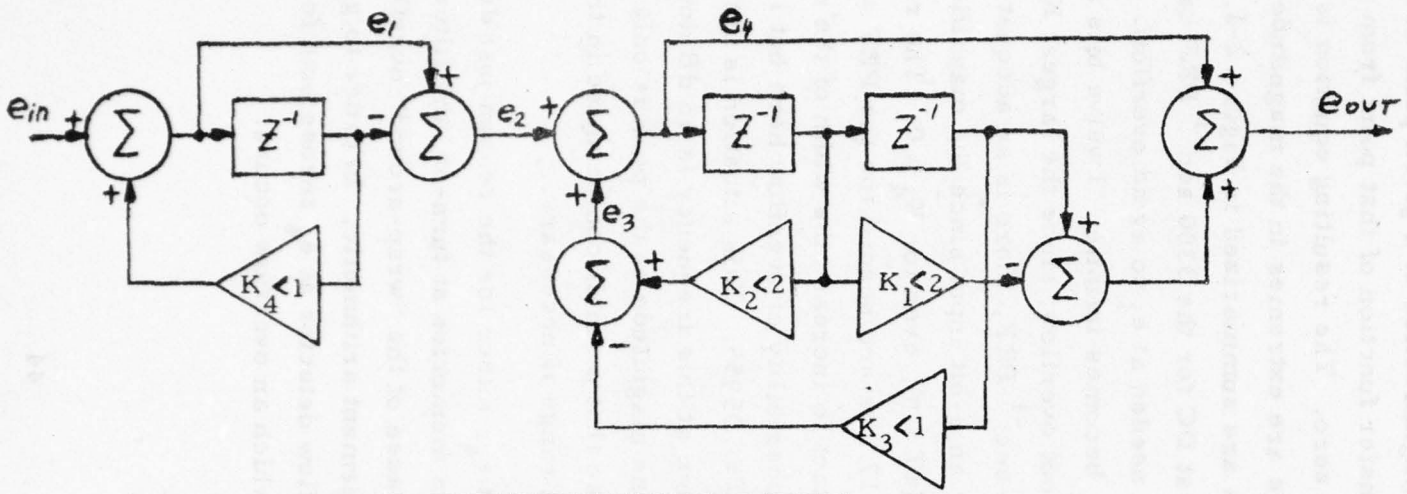
TABLE 2-1. DIGITAL CANCELLER REQUIREMENTS

Number of Channels:	2 (I & Q)
Number of Range Gates:	1024
Min. Time/Gate:	0.5 μsec
Inputs:	7 bits + sign
Memory (both channels):	98,304 bits
Arithmetic Unit (both channels):	
8 multiplies (16 x 16)	per range gate
12 adds	per range gate
6 memory reads	per range gate
6 memory writes	per range gate
16 bit fixed-point arithmetic	

2.1 Magnification and Overflow Considerations

In infinite impulse response or recursive sampled-data filters (those having feedback), it is possible for variables within the filter to grow in magnitude to values many times that of the input, even though the overall transfer gain is less than unity. In a digital implementation of such a filter, an adequate number of bits must be allocated for each variable so as to prevent internal overflow which can cause catastrophic instability.

The three-pole elliptic filter described in Reference 1 is redrawn (Figure 2-1) using two-input adder/subtractor units and with the same topology as the network of hardware arithmetic and memory elements to be described later. The four coefficients have been evaluated for a transmitter frequency of 3200 MHz and a notch width of 0.32 m/sec for PRF's



SIGNAL	MAGNITUDE e/ein=1	@ωT=	WITH CONSTANTS FOR PRF = (see Ref. 1.)
e_1	9.18	0	3300 Sec^{-1}
e_2	1.057	π	3300
e_2	1.36	π	525
e_2	2.	π	- $K_4=0$
e_4	281.	.05955	3300
e_4	10.5	.371	525
e_3	≈ $\|e_4\|$		
e_{OUT}	0.931	π	3300
e_{OUT}	0.867	π	1630
e_{OUT}	0.779	π	917
e_{OUT}	0.651	π	525

Figure 2-1. Three-Pole Elliptic High-Pass Filter

of 525, 917, 1630 and 3300 sec^{-1} (Table 1 of Reference 1). While these sets of constants will not necessarily be the ones stored in the canceller's constant ROM, they are representative enough to use in a magnification analysis.

In order to determine the magnification at a given point in the filter, the magnitude squared of the transfer function of that point from the input is differentiated and set equal to zero. The resulting equation is solved for the frequencies at which there are extremes in the magnitude squared function. The significant results are summarized in Figure 2-1. At e_1, the maximum magnitude is 9.18 at DC for the 3300 sec^{-1} PRF case; thus, if the input is 8 bits, 12 bits are needed at e_1 to avoid overflow. Obviously, as $K_4 \rightarrow 1$ the magnification at e_1 becomes infinite. Twelve bits at e_1 allow K_4 to be as large as 0.9375 without overflow; since the largest K_4 in Table 1 of Reference 1 is 0.891 for 3300 sec^{-1} PRF, there is an adequate margin. At e_2, only 9 bits are needed for an 8-bit input since the magnification only approaches two at half the PRF ($\omega T = \pi$), even for $K_4 = 0$. The real problem is at e_4, a memory input where 17 bits are needed for the PRF = 3300 sec^{-1} case. Since we are reluctant to increase the width of the memory word beyond 16 bits, there is a possibility of overflow here but it would take a full amplitude signal at $\omega T = .05955$. This situation is extremely unlikely since the clutter spectrum at this frequency is 45 dB down from its maximum at DC. Besides, the magnitude at the peak is only 10% too large to be handled with 16 bits so that a small compromise in the values of K_2 or K_3 could bring it within range if necessary.

Should an overflow occur at e_4, either for the reason just discussed or because of random numbers in the memories at turn-on, the filter could exhibit non-linear oscillation because of the "wrap-around" overflow characteristic of the two's-complement arithmetic. In order to guard against such a disaster, an overflow detector at e_4 zeroes both following memories for any range cell in which an overflow occurs.

2.2 Module Interconnection

The Digital Filter Module (DFM) card performs all of the operations indicated in Figure 2-1 for a range-cell interval of two microseconds. Thus, four time-multiplexed DFMs each are needed for the I and Q channels in order to process 0.5 microsecond range cells. The initial canceller has only four DFMs, hence, it can only handle 1 or 2 microsecond cells; however it can be expanded by the addition of four DFMs.

Figure 2-2 reveals how the DFM are interconnected; each block represents an Augat wire-wrap panel. The TIC (Timing and Interface Controller) card, to be described in SECTION 4, generates clocks, control signals, memory addresses and coefficients distributed on busses to all of the DFM. The TIC, together with four or eight DFM, is located in a panel rack designated "T" (top) which is mounted on hinges above rack "R" (rear) in the PPP.

All connections between the canceller in rack "T" and the PPP itself pass through a connector at the top of the PPP 20 Canceller Interface card, added to the PPP in slot F7. This card contains two identical arrays of shift registers, one for the I channel and one for Q, which perform the needed parallel/serial conversion of the PPP's A/D converter outputs, the time multiplexing of range cells among the DFMs, and serial/parallel conversion of the DFM outputs.

The wiring of the backplane of rack "T" and the connector to PPP 20 are described by the wire list included as Appendix A. Extensive use of twisted-pair transmission lines was required because of the high clock rates involved in the serial arithmetic circuits.

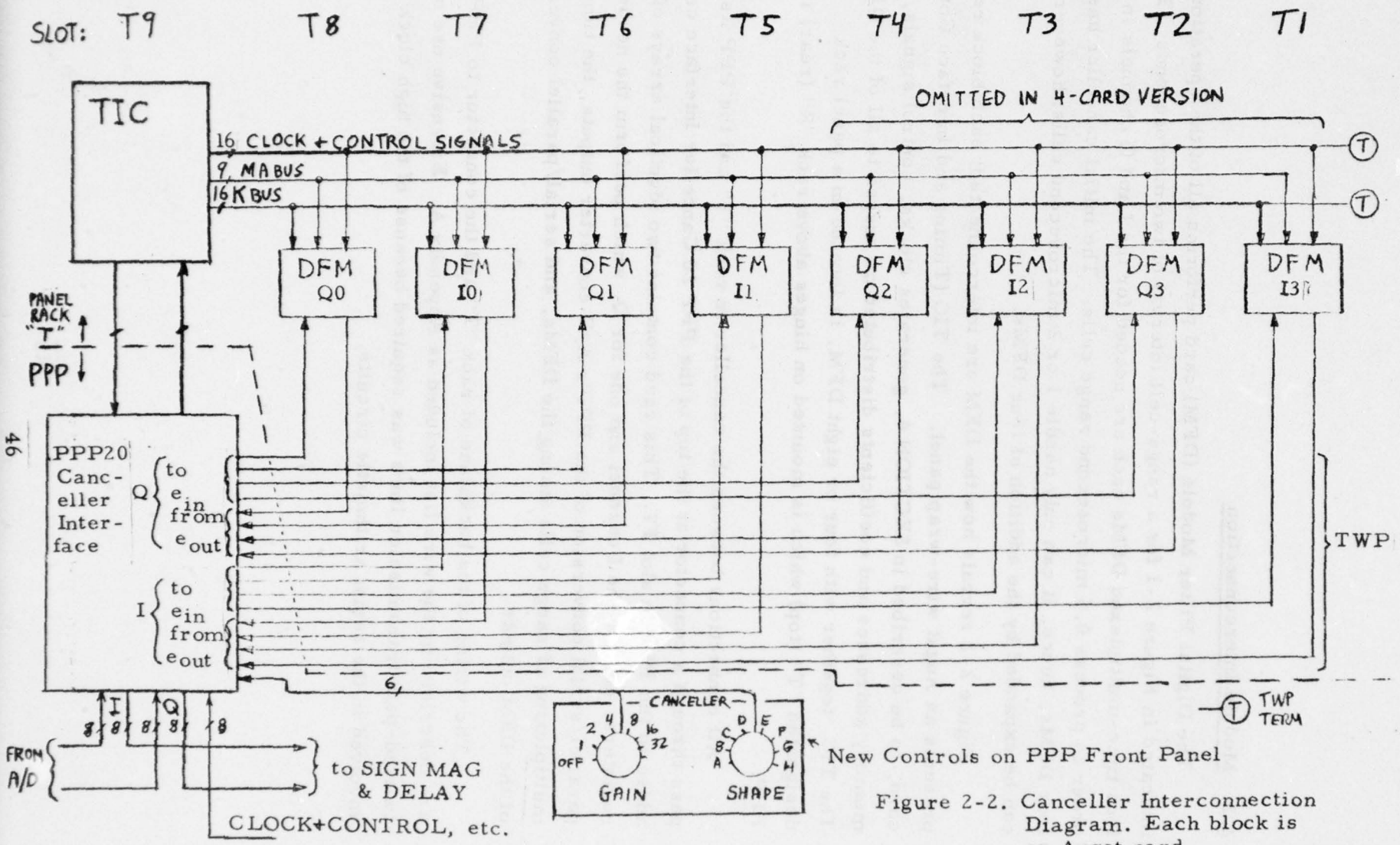


Figure 2-2. Canceller Interconnection Diagram. Each block is an Augat card.

SECTION 3. OPERATION

Two controls, pictured in Figure 2-2, have been added to the PPP front panel. When the CANCELLER GAIN switch is in its OFF position, the canceller is bypassed on the PPP 20 card; however, the PPP still benefits from the crystal-controlled clock on the TIC card. If the connector to the top of the PPP 20 card in F7 is removed, the PPP still operates but uses its own internal delay line clock. The PPP will not operate with PPP 20 removed.

To use the canceller, select the desired GAIN and SHAPE switch positions*. The gain settings are relative and depend on the particular set of constants as described in Reference 1, but in general a GAIN switch setting of 1 means that doppler components in the passband have about 0.6 to 0.9 amplitude compared with the canceller-off case. The important parameters of each of the eight sets of constants, as initially programmed, are summarized in Table 1 of Appendix B, while a frequency response plot for each set is included in Appendix C. Notch width increases (hence settling time decreases) monotonically with rotation of the SHAPE switch clockwise toward H. The constants are stored in two programmable Read-Only Memories located on the TIC card; the bit patterns and decimal constant values for these PROMS as initially supplied with the canceller are listed in Appendix D.

*If the "T" rack only contains 4 DFMs, be sure that 0.5 μs cell width is not selected.

SECTION 4. DETAILED CIRCUIT DESCRIPTION

Each of the following subsections describes a major element of the canceller in terms of block diagrams and timing charts included in this report. Additional, more detailed information is contained in Appendices D and E (PROM Patterns), Appendix F (Summary of Card Indexing), and in the schematic diagrams referenced in Appendix G.

CAUTION

The 2606 memory devices used on the DFM cards are MOS and therefore require normal MOS handling precautions (storage in conductive foam, etc.) to prevent damage due to static discharge.

4.1 The Digital Filter Module

Serial, two's-complement, LSB-first arithmetic has many advantages in implementing a digital filter module for a processor such as a canceller where identical operations are performed on successive range cells and there is no cell-to-cell information transfer. In this type of processor, it is very straightforward to multiplex the modules, simple but slow because they use serial arithmetic, to obtain the required processing rate. This section describes a module which implements the filter presented in Figure 2-1 with a throughput rate of one range cell per two microseconds. The next section shows how eight such modules can be multiplexed to yield the required rate of two range cells per microsecond for both I and Q channels (the eight-card version) or how four modules can yield a compromise rate of one cell per microsecond (the four-card version).

A block diagram of the DFM appears in Figure 4-1. Four adder/subtractor units are available in each Am25LS15, thus only two of these packages are needed for the six operations in the DFM. Serial adders are extremely simple to implement in hardware using LSB first two's complement arithmetic; greater precision can be achieved with no additional hardware by simply allowing more time which includes more cycles of the bit clock hence more bits in the arithmetic representation. But adders alone do not justify using serial arithmetic; the key reason is the availability of the Am25LS14 eight-bit serial/parallel two's complement multiplier. Only eight of these low-power Schottky devices are required to perform the four 16 x 16 multiplications required in the DFM. By using the parallel (multiplicand) inputs for the four coefficients, available on a time-multiplexed basis from a 16-bit K bus common to all of the DFM, the serial inputs (multiplier) and outputs (product) are compatible with the economical serial adders.

The remaining consideration is memory; 16-bit words for each of 512 range cells required in the four-card version would require an 8192 bit shift register which isn't particularly a problem except that we need a bit clock frequency of about 20 MHz in order to achieve a one-cell per two microsecond throughput rate with the required 16-bit precision. Since long MOS shift registers do not have adequate speed, we would be forced to use bipolar shift registers which are not available in lengths greater than about 16 bits/package. Fortunately, there are alternatives to using one IC package of memory for each range cell. Along with the serial adder and multiplier, Advanced Micro Devices has provided us with the Am25LS22 eight-bit serial/parallel register with sign extend. This device, having eight terminals which can serve either as parallel inputs or outputs, is extremely versatile and can perform serial-to-parallel, or parallel-to-serial conversions with the sign-extend feature required by the multiplier input.

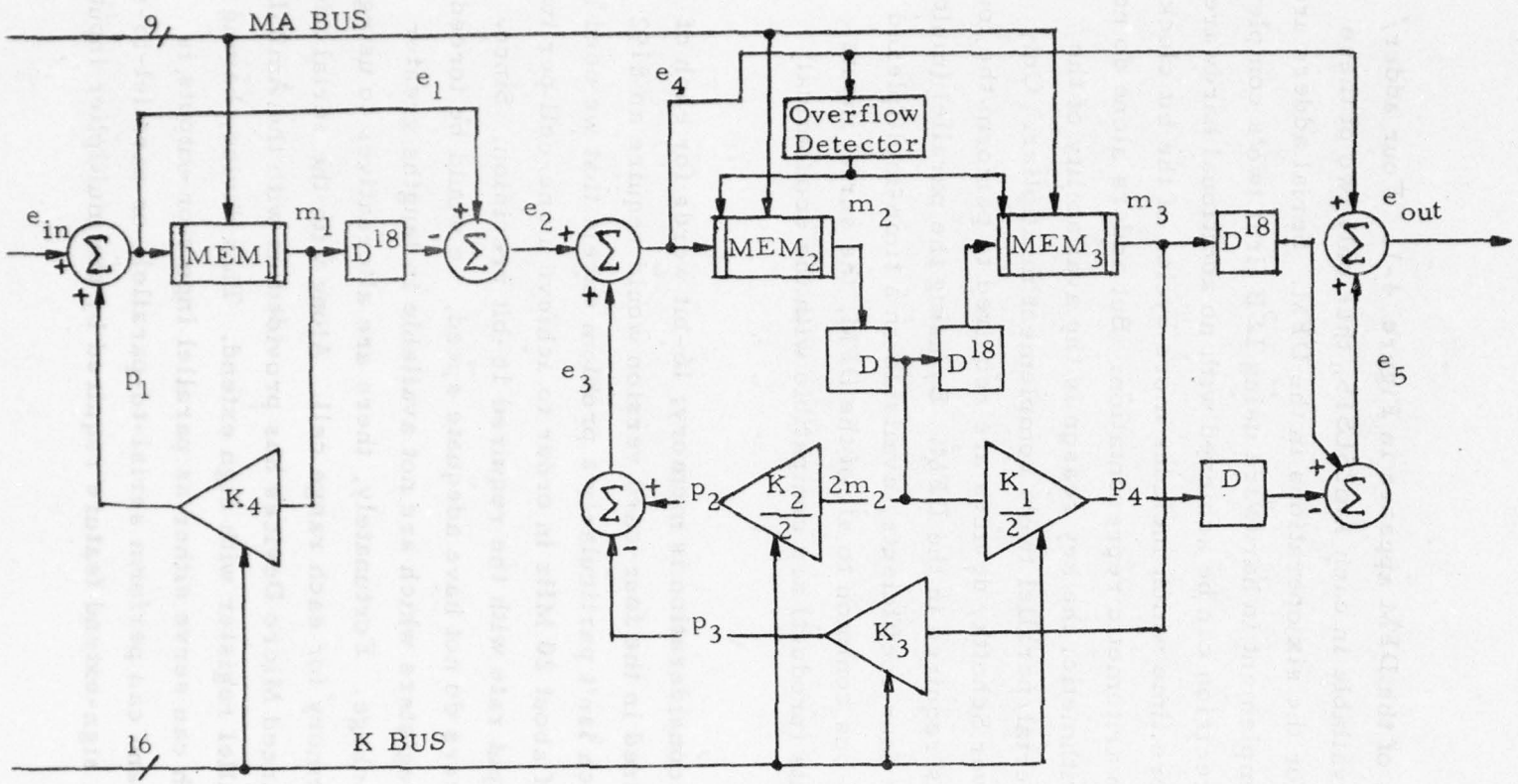
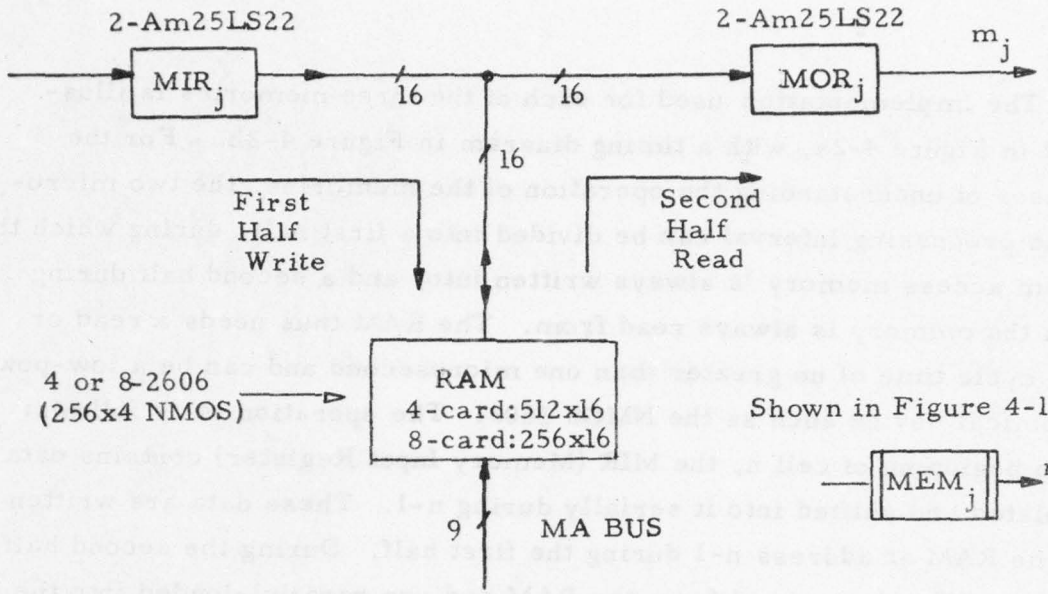


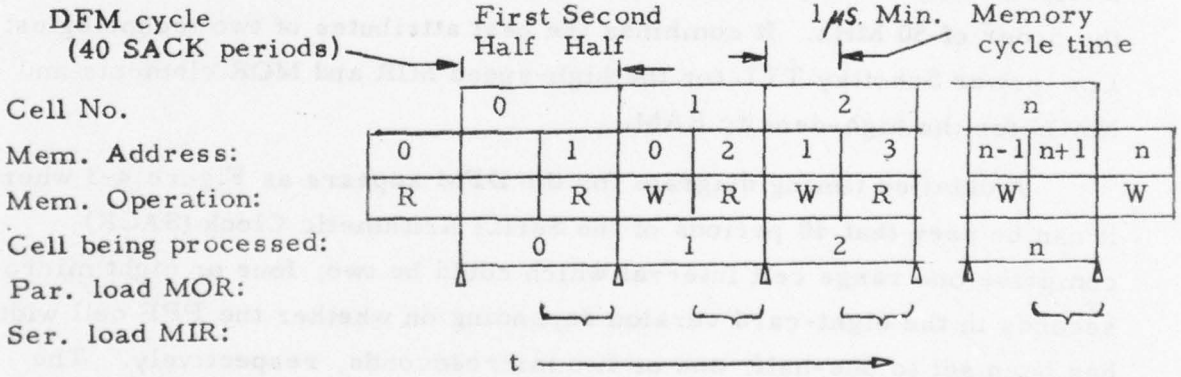
Figure 4-1. DFM Block Diagram

The implementation used for each of the three memories is illustrated in Figure 4-2a, with a timing diagram in Figure 4-2b. For the purposes of understanding the operation of the memories, the two microsecond processing interval can be divided into a first half, during which the random access memory is always written into, and a second half during which the memory is always read from. The RAM thus needs a read or write cycle time of no greater than one microsecond and can be a low-power economical device such as the NMOS 2606. The operation is as follows: At the beginning of cell n, the MIR (Memory Input Register) contains data calculated and shifted into it serially during n-1. These data are written into the RAM at address n-1 during the first half. During the second half, data for cell n+1 are read from the RAM and are parallel-loaded into the MOR near the end of the cycle. These data are available for serial output during cell n+1. Also during the second half, data calculated in the arithmetic elements are shifted serially into the MIR. This scheme emulates an 8192 bit shift register (or one with some lesser multiple of 16 bits) using a total of only 12 IC packages and capable of operation at clock rates of the order of 50 MHz. It combines the best attributes of two technologies: Low-power Schottky TTL for the high-speed MIR and MOR elements and NMOS for the high-density RAM.

A detailed timing diagram for the DFM appears as Figure 4-3 where it can be seen that 40 periods of the Serial Arithmetic Clock (SACK) comprise one range cell interval which could be two, four or eight microseconds in the eight-card version depending on whether the PPP cell width has been set to one-half, one or two microseconds, respectively. The maximum frequency of SACK is thus 20 MHz, which leaves a comfortable margin since the minimum F_{max} for the 25LS14 multiplier is 25 MHz, while it is 30 and 50 MHz for the 25LS15 adder and the 25LS22 register, respectively.



(a) Block Diagram of one of the three memories.



(b) Simplified Memory Timing.

Figure 4-2. Memory Organization and Timing

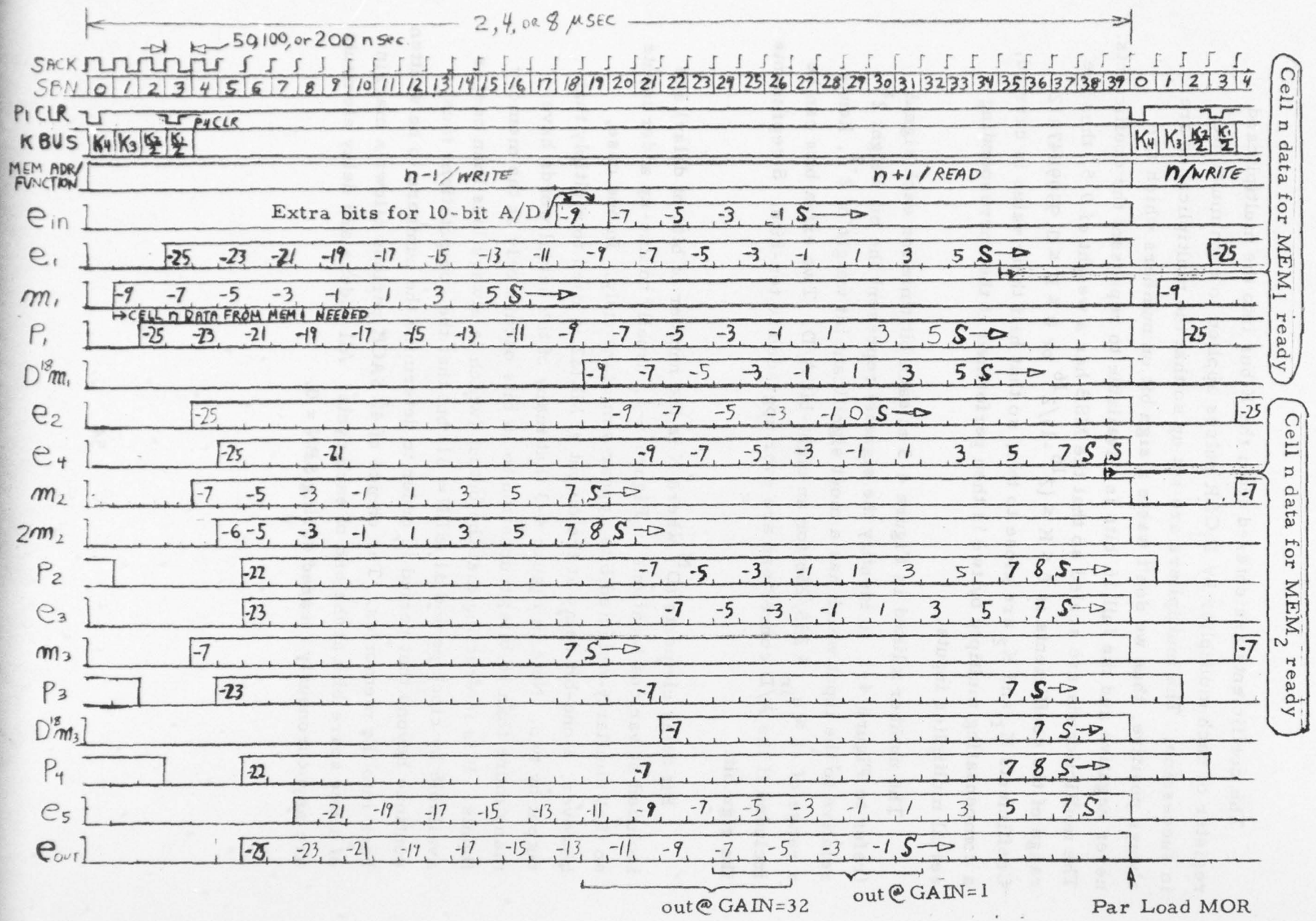


Figure 4-3. DFM Timing. The numbers x listed for each signal indicate the bit weight 2^x relative to the input ($-1 \leq e_{in} < 1$).

The coefficients are entered from the K bus into the multiplicand register of each multiplier by P_jCLR pulses applied to each multiplier in succession. The multipliers are set up so that the multiplicands are always positive, thus we don't waste a sign bit on numbers which are never negative and the full 16 bits is available to represent the coefficients. The multiplicands are scaled so that the MSB has a weight of 0.5, thus the range of the coefficients is $0 \leq K \leq (2^{16}-1)/2^{16}$ or $0 \leq K \leq 0.9999847412$. Coefficients K_1 and K_2 are close to two, so that half their value is carried; a compensating multiply by two is then performed at the corresponding serial multiplier inputs.

The number x listed in Figure 4-3 at each bit time for each signal (refer to Figure 4-1 to identify the signals) represent the bit weight 2^x relative to the input which has a most significant bit weight of 2^{-1}, hence a range of $-1 \leq e_{in} \leq 255/256$ for an eight-bit A/D. Two extra bits can be included if the A/D converters are ever upgraded to ten-bits. S represents the sign bit.

Bit delay elements (D^N where N is the number of bits of delay) are included at various locations in Figure 4-1, usually to line-up adder inputs so that similarly-weighted bits appear simultaneously. In one case, however, a one-bit delay at the output of MEM2 is used to multiply that output by two. Note in Figure 4-3 that many of the serial words have many more than 16 bits; truncation to 16 bits occurs only at the memory inputs. It is interesting that the output (which is always less than one) is available by clock period 31 (SBN = 31) but that the computations must continue beyond that period in order to determine the numbers to be written back into the memories. The choice of 40 SACK periods allows a margin of a few spare bits at the end of each cycle. All adders and delay elements are asynchronously cleared during SBN = 0.

An overflow detector connected to e_4 determines that an overflow condition exists by responding to the condition of e_4 having different states during SBN = 38 and SBN = 39 (Figure 4-3). When such an abnormal condition is detected, memory input registers MIR2 and MIR3 are forced to zero for the particular cell in which the violation occurred. This precaution eliminates the problem of non-linear oscillation which could arise from either random numbers in the memories at power turn-on or an actual overflow resulting from an abnormally high amplitude response at e_4.

4.2 Canceller--PPP Interface

It is apparent from Figure 4-3 that the throughput delay of the DFM, allowing for eight-bit parallel/serial and serial/parallel conversions at the input and output, is 12 SACK cycles or 600 nsec at the fastest clock rate. Unfortunately, such a delay will upset the timing of the PPP. It is possible to arrange the timing of the DFM's so that each of the four sets of I & Q modules is offset in time by 500nsec so that the first range cell goes to modules I0 and Q0, the second to I1 and Q1, and so on. With this arrangement, the 600 nsec delay is equivalent to two 0.5 μsec range gates with 400 nsec margin. However, not only does the PPP timing have to be altered to accommodate two more cells worth of delay in the AGC loop (Reference 3), but there are four different sets of serial arithmetic and memory timing (Figure 4-3) to contend with.

The approach used in the ground clutter canceller is described in Figure 4-4. The serial/parallel/serial arrangement accumulates four input samples in the Input Register (IR) then parallel loads the four Parallel In/Serial Out Registers (PISOR) which are subsequently simultaneously shifted out to supply serial inputs to the four DFMs. The inverse operation

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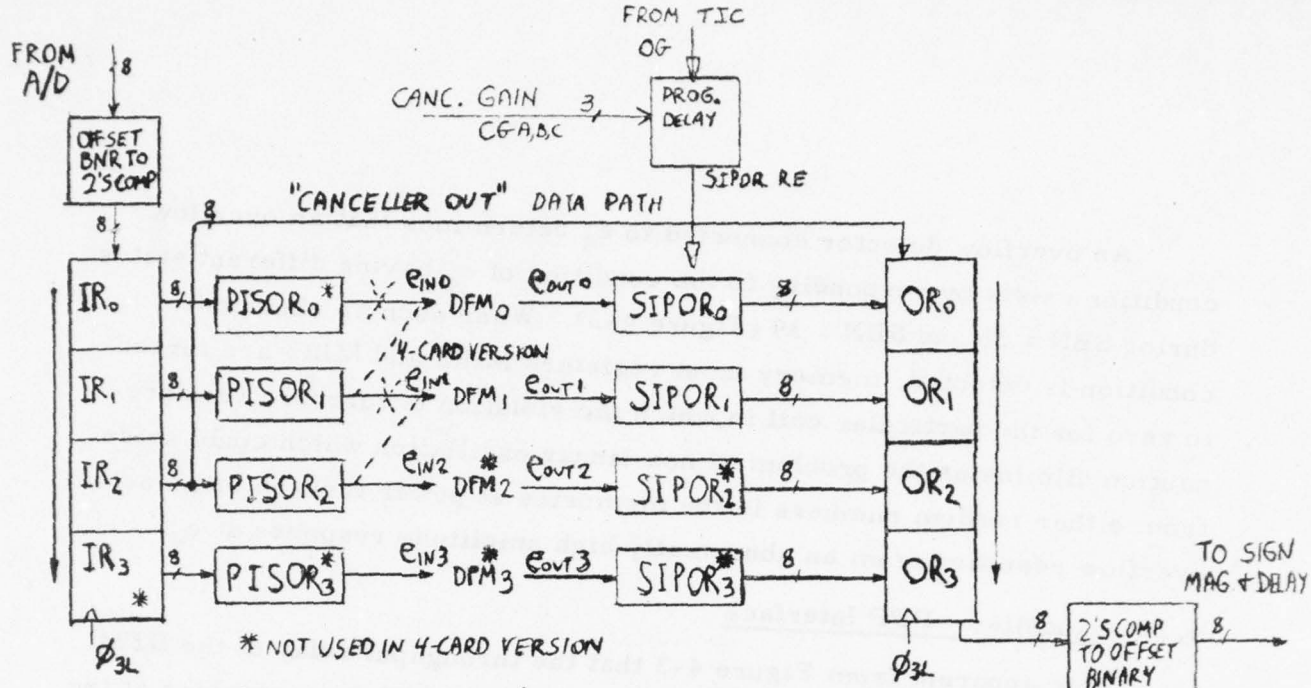
Reference 3. "Pulse Pair Processor Equipment Information Report" F19628-72-C-0293, May 1974.



I CHANNEL PS/SP CONVERTER ON PPP20
(Q CHANNEL IS IDENTICAL)

	t → 8-CARD VERSION → ← 0.5, 1, or 2 μs															t → 4-CARD VERSION → ← 1 or 2 μs													
RCELL NO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
LOAD PISOR LOAD OR	▼			▼			▼			▼			▼			▼		▼		▼		▼		▼		▼		▼		
																1 or 2 ONLY														
A/D OUT	A	B	C	D	E	F	G	H	I	J	K	L	M			A	B	C	D	E	F	G	H	I	J	K	L	M		
IR 0		A	B	C	D	E	F	G	H	I	J	K	L	M			A	B	C	D	E	F	G	H	I	J	K	L	M	
1			A	B	C	D	E	F	G	H	I	J	K	L	M			A	B	C	D	E	F	G	H	I	J	K	L	M	
2				A	B	C	D	E	F	G	H	I	J	K	L				A	B	C	D	E	F	G	H	I	J	K	L	
3					A	B	C	D	E	F	G	H	I	J	K																
DFM 0 INPUT						D				H					L					A		C		E		G		I		K
1						C				G					K							B		D		F		H		J
2						B				F					J															
3						A				E					I															
OR 0								D'	E	F	G	H'	I	J	K						A'	B	C'	D	E'	F	G'	H	I'	J	K'
1								C'	D'	E	F	G'	H'	I	J							A'	B'	C'	D'	E'	F'	G'	H	I'	J'
2								B'	C'	D'	E	F'	G'	H'	I								A'	B'	C'	D'	E'	F'	G'	H'	I'
3								A	B'	C'	D'	E'	F'	G'	H'									A'	B'	C'	D'	E'	F'	G'	H'
	← 7 CELL DELAY →															← 7 CELL DELAY →														

Figure 4-4. Shift Register Array

is performed by the SIPOR's and OR's at the output. The net delay is equivalent to seven range cells. In the four-card version, the simple changes indicated by dashed lines are made to retain the seven-cell delay. With the canceller turned off or removed, the data samples flow through the "CANCELLER OUT" data path and the array functions simply as a seven-cell shift register so that the PPP, with timing modified to accommodate this delay, can operate normally.

A new card, PPP20 (Canceller Interface) containing two of the Register arrays described in Figure 4-4 (one for the I channel and one for the Q) plugs into formerly vacant slot F7 of the PPP front panel rack. A variable delay unit, controlled by the CANCELLER GAIN switch added to the PPP front panel, allows selection of various canceller gains in powers of two by sampling e_{out} (Figure 4-3, bottom) at different times. PPP20 also performs code conversions between offset binary and two's complement arithmetic.

The top of PPP20 is fitted with a connector which mates with a cable wired to the T backplane. All signals between the PPP and the canceller, including the serial DFM inputs and outputs, pass through this cable. When it is disconnected to remove the canceller, the PPP can function normally with A/D outputs passing through the "CANCELLER OUT" data paths (Figure 4-4).

4.3 The TIC Card

The Timing and Interface controller card block and timing diagrams appear as Figure 4-5. The three-bit code CS, from an eight-position CANCELLER SHAPE control added to the PPP panel (Figure 2-2), selects one of eight sets of coefficients stored in the K ROM, a 32 x 16 programmable read-only memory. Programming for the two PROMs which comprise this memory is described in Appendix D which lists not only the binary codes but also the decimal values of the constants as calculated from the binary codes. Other sets of constants can be obtained by similarly

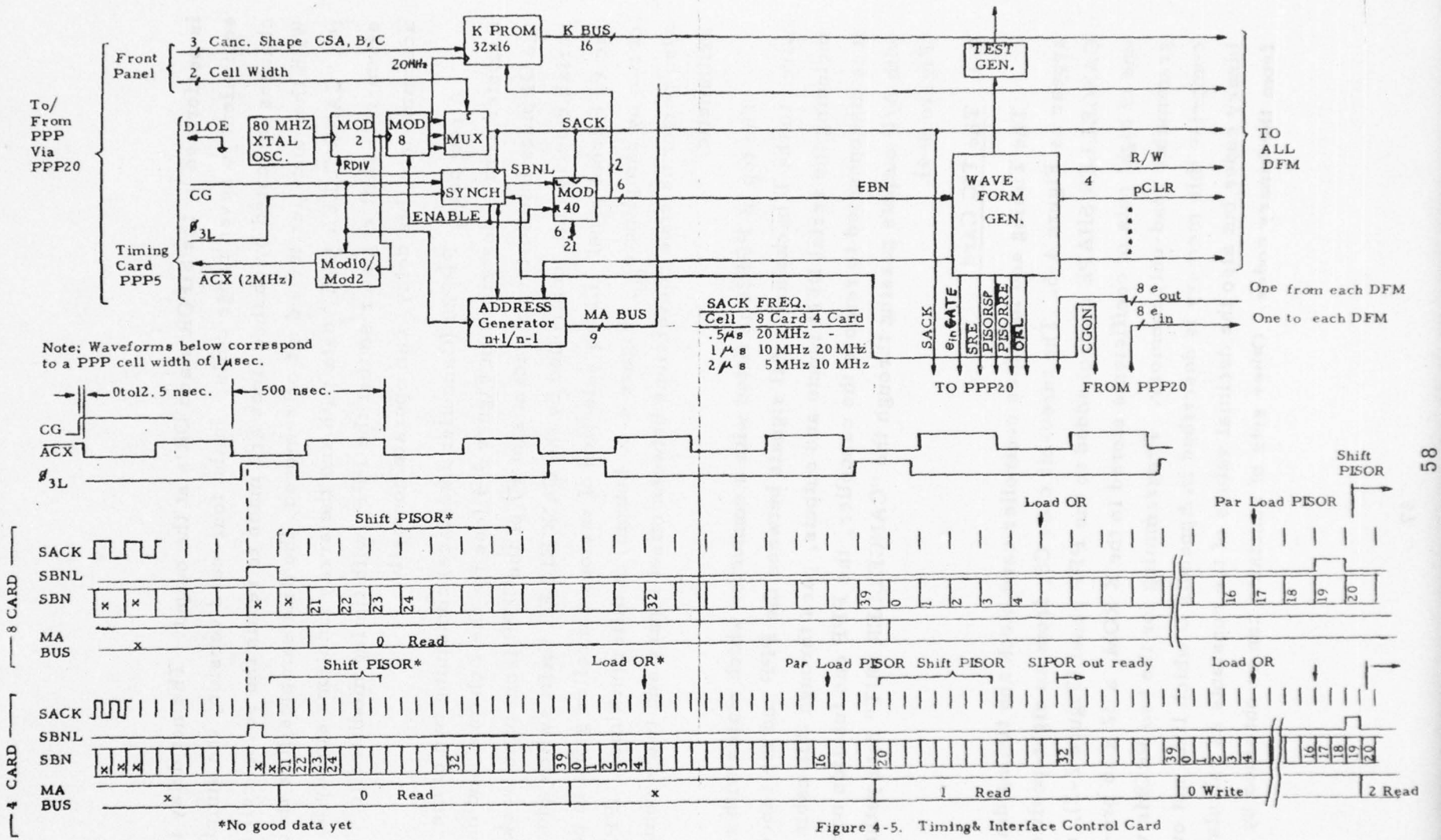


Figure 4-5. Timing& Interface Control Card

programming pairs of Signetics N82S123B devices. The remaining two address inputs are driven by the two least significant bits of the Modulo 40 EBN counter such that, after passing through a register clocked by a 20 MHz clock, the constants appear on the K BUS as indicated in Figure 4-3. The constants repeat this cycle ten times during each 40 bit cycle, but only the values during SBN 0, 1, 2, and 3 are important since the P_jCLR occur during these times.

All timing for the canceller and for the PPP when the canceller is connected is derived by frequency division of the output of an 80 MHz crystal-controlled oscillator as shown in Figure 4-5. Modifications to the PPP5 "Timing and Dump Generator" allow the PPP to use its existing delay line oscillator when the canceller is disconnected (DLOE = High), or the two-MHz $\overline{ACX}$ signal from the TIC when it is connected. In the latter case, when the CG signal from PPP5 goes high following a radar trigger, a narrow pulse RDIV resets the MOD2 counter thereby setting the phase of its 40 MHz output, while the MOD 10/MOD2 counter is allowed to generate the $\overline{ACX}$ waveform for the PPP (see timing diagram in Figure 4-5). These operations take place whether or not the canceller has been switched on. Because of the high clock frequency, the timing jitter is only $\pm$ .5/80 MHz or $\pm$ 6.25 nsec, while the timing accuracy over many range cells is far superior to that obtainable with the PPP's delay line oscillator.

Since the PPP clock rates vary with cell width as selected from the front panel, the same method is used in the canceller but the multiplexer used to accomplish this switching must be wired differently (see "SACK FREQ." table in Figure 4-5), depending on whether a four or eight card version is in operation. In any case, the frequency of the serial arithmetic clock SACK ranges from 5 MHz to 20 MHz, as developed by the MOD8 counter and selected by the MUX.

In the PPP5 card, the various clock phases are developed using monostable analog delay elements. The only clock phase of concern to the canceller is the leading edge of ϕ_{3L} which clocks the IR and OR on PPP20

and which indicates that the A/D outputs are valid. In order to minimize the effects of timing variations in ϕ_{3L} with respect to $\overline{ACX}$ caused by variations in the monostables on PPP5, the synchronization scheme shown in Figure 4-5 has been used. Every fourth ϕ_{3L} edge generates an SBNL pulse beginning at the next SACK positive transition. SBNL, in turn, sets the MOD40 counter to state EBN = 21 at the next SACK transition so that SBN becomes 21 after one more SACK transition (see examples in Figure 4-5). Note that at any given time the state of the MOD40 counter, EBN, is one ahead of SBN, the Serial Bit Number to which all arithmetic timing is referenced. Once synchronized, the various load or shift events and memory-address changes occur at the proper times as indicated at the bottom of Figure 4-5, where examples for both 4 and 8-card versions are shown with a one-microsecond cell width selected.

The address generator develops the n + 1, n - 1 sequence of addresses as described in Figure 4-2. The selection of various numbers of cells processed in the PPP will not need to be taken into account since CG will go low when that number has been reached; everything is then reset and ready for the next radar trigger. The only problem is when "1024 cells processed" has been selected. Because of timing changes to the PPP described in the next section, the last eight cells would exceed the memory capacity of the canceller. The solution is to disable the canceller by turning off the load commands to the OR's on PPP20, thereby permitting data to flow through the "CANCELLER OUT" path (Figure 4-4), in this case. The canceller thus does not operate on the last eight range cells when "1024 cells processed" has been selected. The same mechanism is used to disable the canceller when the CANCELLER GAIN switch is in its OFF position (CG ON = low).

The functions just described are combined in the SYNCHronizer (Figure 4-5) which generates the ENABLE signal. When ENABLE is low, only those counters necessary for non-canceller PPP operation are allowed to run and $\overline{ORL}$ is forced high so that data flow through the

"CANCELLER OUT" path on PPP20. Within the synchronizer but not shown in Figure 4-5 are two signals, NORE and OVFE which are anded to form ENABLE. If other than "1024 cells processed" has been selected on the PPP panel, OVFE stays high and NORE (hence ENABLE in this case) is asynchronously set when CG goes high. After CG goes low, NORE stays high until the next SBN = 20 so that the last memory write operation can be completed. If "1024 cells processed" has been selected, NORE stays high and OVFG (hence ENABLE in this case) goes low when the write address counter has reached its limit. OVFG is synchronously set when CG goes high. If CG ON is low (canceller switched OFF), then NORE is held low to disable the canceller.

The Address generator is composed of a Write counter and a Read counter, initialized to two different starting values and multiplexed onto the MA BUS so as to generate the sequence of addresses required (see Figures 4-2 and 4-5). Starting values are loaded by $\overline{\text{LDAC}}$ which goes high after ENABLE at the beginning of each radar period. The first Write operation is inhibited by a signal called $\overline{\text{BWR}}$ so that bad data do not over write the last range cell if "1024 cells processed" has been selected.

In addition to the P_1CLR - P_4CLR signals already mentioned (see Figure 4-3), a number of timing signals both for the DFMs and PPP20 are generated by the TIC. The waveforms, illustrated in Figure 4-6, are developed using PROMS addressed by EBN with outputs registered and buffered. The PROM patterns are included as Appendix E.

The TIC card also includes a test waveform generator which provides signals convenient for troubleshooting the canceller (see schematic). Eight different serial words representing points on a sinusoid are stored in PROM U35 (L26). One of these waveforms, as selected by an eight-input multiplexer, can be made to appear on pin 119 ($\overline{e_{in}}$ TEST OUT) with timing compatible with the DFM inputs. Another PROM, U54 (N44), drives the select and enable lines of the multiplexer and is itself addressed by a four-bit binary counter. A jumper selects sinusoidal or square-wave

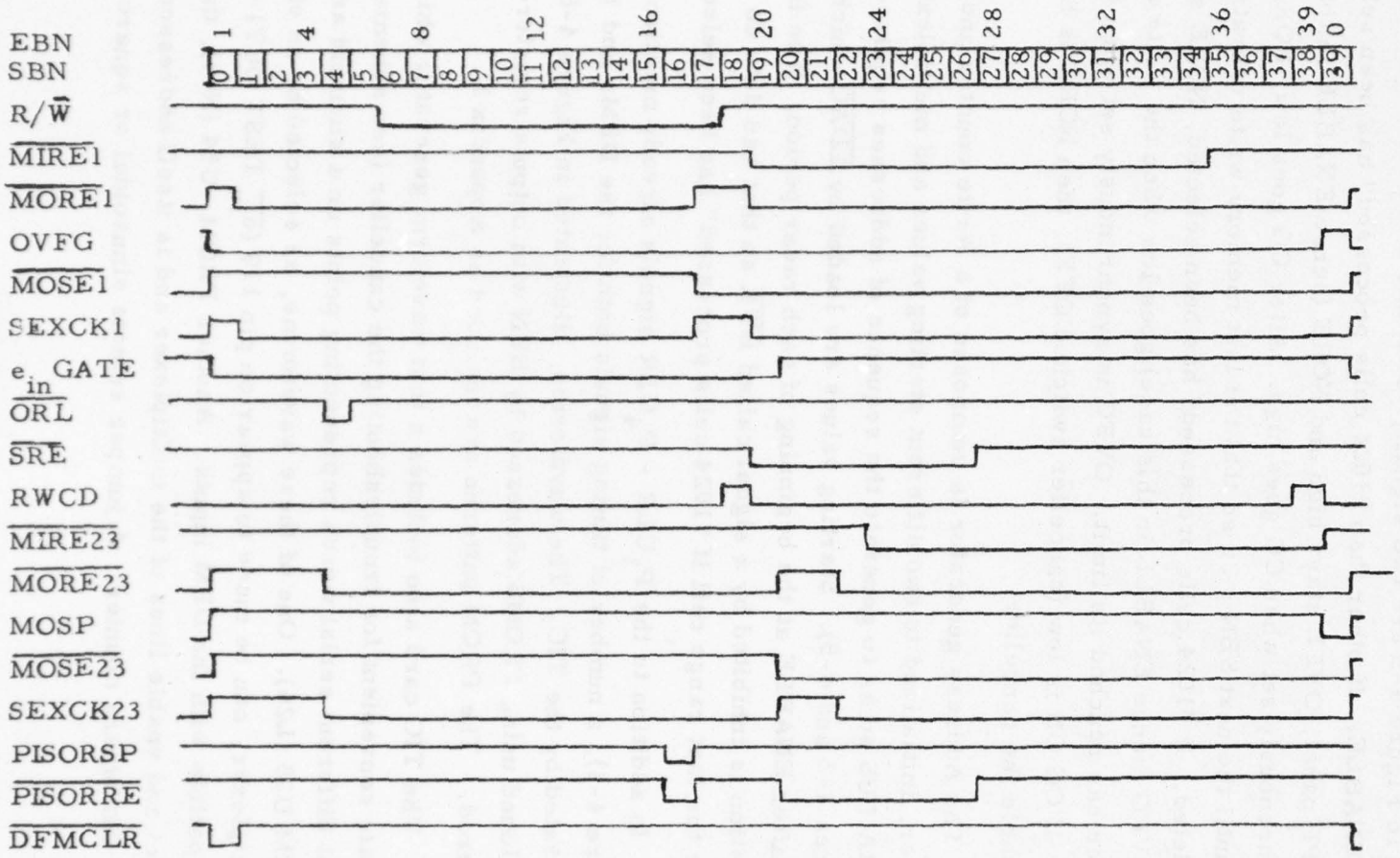


Figure 4-6. Arithmetic Timing Waveforms

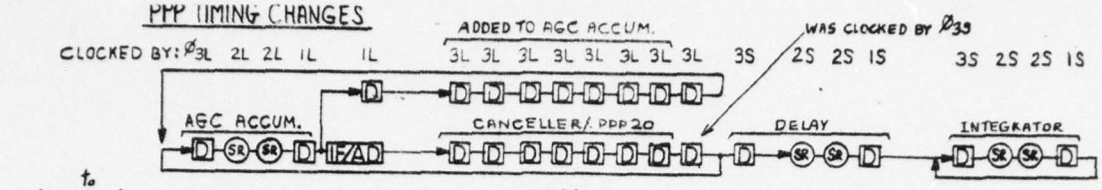
functions by selecting the lower or upper addresses of U54. The binary counter can be jumpered to either count once every 2 μsec or to serve as a register for a second four-bit binary counter which drives its inputs. This second counter can be incremented by applying a clock pulse to pin 117 (PA CLK TEST INPUT). The tester can be used to simulate signals which vary either from cell-to-cell or from period-to-period or both.

4.4 PPP Modifications

Modifications which have been performed on the PPP, many of which have been mentioned in preceding sections, are summarized in this section. The drawing list in Appendix G contains all PPP drawings which have been revised as a result of these modifications, including the block diagram which shows the addition of the canceller interface after the A/D converter outputs.

In order to compensate for the seven range cells of delay being added after the A/D converters, seven cells of delay had to be added in the 16-bit AGC accumulator loop. This was accomplished by replacing four four-bit registers with eight dual eight-bit 9328 shift registers with a net increase of four IC packages on the PPP6 (AGC Accumulator) card. Seven cells of delay, in the form of seven SN 74273 octal D registers, were also added to the PPP3 card in the power channel. The resulting card, PPP3A, has different indexing from the other PPP3 cards (see Appendix F) since it has added circuitry. The schematic additions and a layout of the revised card are described in a new drawing listed in Appendix G.

The timing and dump generator card needed the most extensive modifications. The gates which control the short and long clocks had to be changed so that after each radar trigger, the short clocks do not turn on until 9 periods of the long clocks have elapsed. Both short and long clocks now end simultaneously. The display trigger had to be correspondingly delayed to line up with the first range cell in the outputs. The effects of these changes have been determined by simulations (Figure 4-7) following



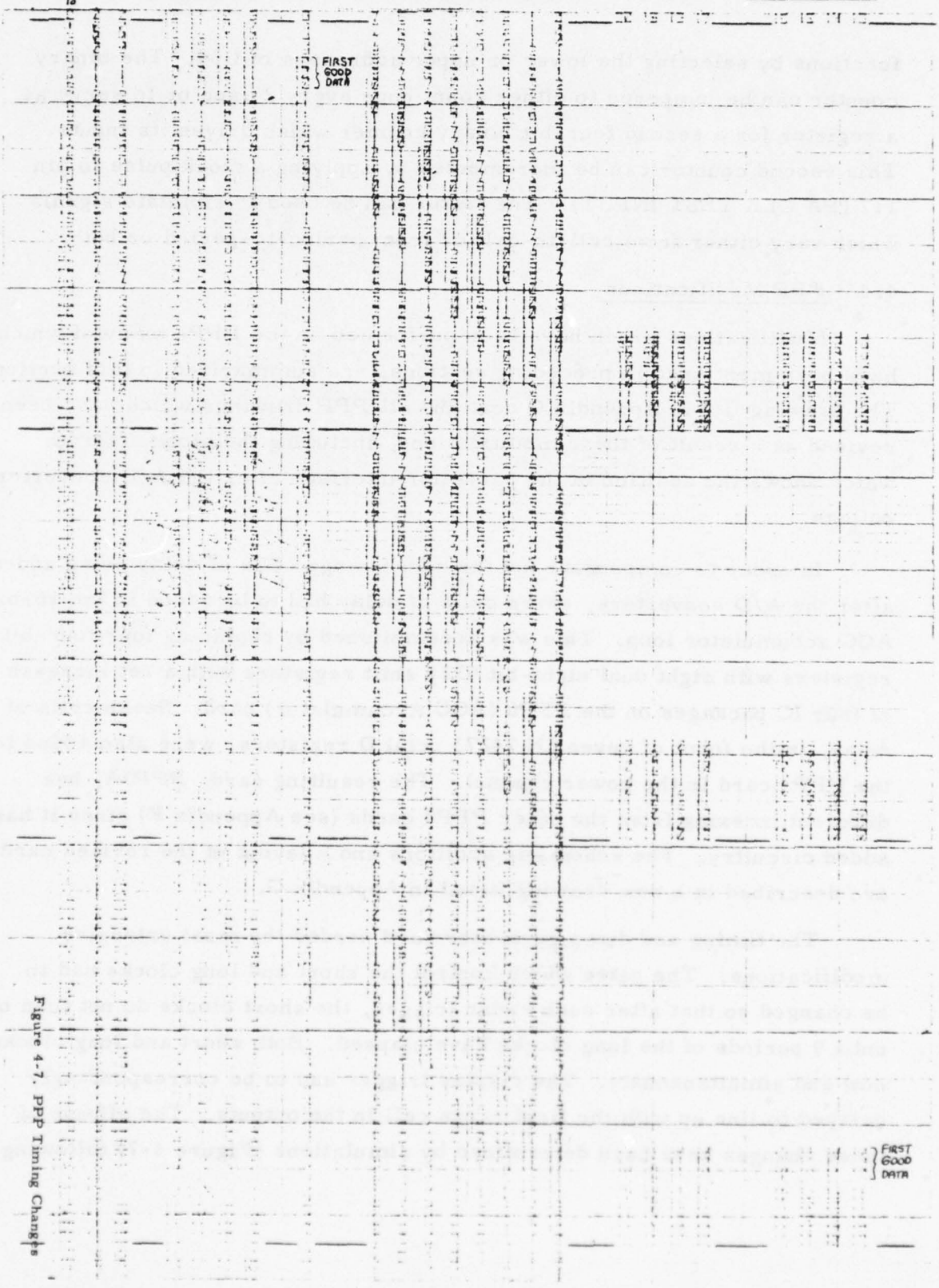


Figure 4-7. PPP Timing Changes

the methods used in Reference 3, Section 5, to be consistent with proper AGC loop timing. PPP5 also has extra inputs and outputs to permit operation from the clocks developed on the TIC card as described in the last section.

The clock driving the input register on the two PPP1 (sign-magnitude and delay) cards has been changed from ϕ_{3S} to ϕ_{3L}. The eight-bit inputs to these cards were rerouted to come from the outputs of PPP20 in slot F7, while the two A/D outputs now connect to the inputs of PPP20.

The wiring of the PPP power supply chassis and its interconnection to the PPP were revised extensively. A new +5 volt Sorensen STM5-36 supply, driving a separate +5 volt bus labeled "+5VC", was added to supply the canceller and to relieve the load on the existing Lambda supply. This new supply provides current for the canceller cards in the T rack (TIC and four DFMs--measured current of 13.7A) and for the PPP simulator. The Lambda supply feeds the PPP itself, the PPP interface, and the PPP20 Card (measured current of 1.55A). These two five-volt busses, "+5V" and "+5VC" are separately remotely-sensed and should not be connected together. All of the DC supply current and sense lines pass through a new power cable which is wired to the PPP but mates with a connector on the power supply chassis.

Mechanically, the T panel rack was mounted on hinges to permit access to the R panel rack below. All signal connections to this rack are through the short cable wired to the "T" backplane and mating with a connector on the top of PPP20. The two canceller controls are rotary switches so that the modifications to the front panel involved simply drilling two 3/8" holes and labeling according to Figure 2-2. Connections to these switches pass through F7 and PPP20 along with all other canceller signals. Power connections, including remote sense for the STM5-36, have been routed separately to a barrier strip on the rear apron.

4.5 Expansion to the Eight-Card Version

As delivered, the canceller has four DFM cards, hence can operate only at cell widths of 1 or 2 microseconds. Provision has been included for expansion to the full eight-card configuration which will allow operation at 0.5, 1 or 2 microsecond cell widths. All necessary registers on PPP20 (see Figure 4-4) have been provided and tested. The four present DFM cards have 512 cells of memory each as opposed to 256 cells in the eight-card version; they therefore contain enough memory for all eight modules. When the four additional DFM cards are constructed, expanding the canceller will simply amount to unplugging half of the memory IC's from the existing cards, inserting them in the new cards*, inserting the new cards in the T panel rack, wiring the four new slots in that rack, and changing a few jumpers on the TIC and PPP20 cards. The additional 5-volt current, estimated at 7 Amps for the four additional DFMs without memories, is well within the capabilities of the STM5-36 supply.

*Observing MOS handling precautions of course.

APPENDIX A

CANCELLER BACKPLANE T WIRING LIST

CANCELLER BACKPLANE T WIRING LIST

Twisted Pairs*				Signal Name	
09-002	to	08-002	level one	K0	(LSB)
09-042	to	08-042			
07-002	to	06-002	level one		
07-042	to	06-042			
08-002	to	07-002	level two		
08-042	to	07-042			
06-002	to	05-002	level two to level one on five		
06-042	to	05-042			

09-003	to	08-003	level one	K1	
09-043	to	08-043			
07-003	to	06-003	level one		
07-043	to	06-043			
08-003	to	07-003	level two		
08-043	to	07-043			
06-003	to	05-003	level two to level one on five		
06-043	to	05-043			

09-004	to	08-004	level one	K2	
09-044	to	08-044			
07-004	to	06-004	level one		
07-044	to	06-044			
08-004	to	07-004	level two		
08-044	to	07-044			
06-004	to	05-004	level two to level one on five		
06-044	to	05-044			
---					

* SLOT # / PIN #

09-002 Signal
09-042 Gnd

Twisted Pairs				Signal Name
09-005	to	08-005	level one	K3
09-045	to	08-045		
07-005	to	06-005	level one	
07-045	to	06-045		
08-005	to	07-005	level two	
08-045	to	07-045		
06-005	to	05-005	level two to level one on five	
06-045	to	05-045		
09-006	to	08-006	level one	K4
09-046	to	08-046		
07-006	to	06-006	level one	
07-046	to	06-046		
08-006	to	07-006	level two	
08-046	to	07-046		
06-006	to	05-006	level two to level one on five	
06-046	to	05-046		
09-007	to	08-007	level one	K5
09-047	to	08-047		
07-007	to	06-007	level one	
07-047	to	06-047		
08-007	to	07-007	level two	
08-047	to	07-047		
06-007	to	05-007	level two to level one on five	
06-047	to	05-046		
09-008	to	08-008	level one	K6
09-048	to	08-048		
07-008	to	06-008	level one	
07-048	to	06-048		
08-008	to	07-008	level two	
08-048	to	07-048		
06-008	to	05-008	level two to level one on five	
06-048	to	05-048		

Twisted Pairs				Signal Name
09-009	to	08-009	level one	K7
09-049	to	08-049		
07-009	to	06-009	level one	
07-049	to	06-049		
08-009	to	07-009	level two	
08-049	to	07-049		
06-009	to	05-009	level two to level one on five	
06-049	to	05-049		

09-010	to	08-010	level one	K8
09-050	to	08-050		
07-010	to	06-010	level one	
07-050	to	06-050		
08-010	to	07-010	level two	
08-050	to	07-050		
06-010	to	05-010	level two to level one on five	
06-050	to	05-050		

09-011	to	08-011	level one	K9
09-051	to	08-051		
07-011	to	06-011	level one	
07-051	to	06-051		
08-011	to	07-011	level two	
08-051	to	07-051		
06-011	to	05-011	level two to level one on five	
06-051	to	05-051		

09-012	to	08-012	level one	K10
09-052	to	08-052		
07-012	to	06-012	level one	
07-052	to	06-052		
08-012	to	07-012	level two	
08-052	to	07-052		
06-012	to	05-012	level two to level one on five	
06-052	to	05-052		

Twisted Pairs				Signal Name
09-013	to	08-013	level one	K11
09-053	to	08-053		
07-013	to	06-013	level one	
07-053	to	06-053		
08-013	to	07-013	level two	
08-053	to	07-053		
06-013	to	05-013	level two to level one on five	
06-053	to	05-053		

09-014	to	08-014	level one	K12
09-054	to	08-054		
07-014	to	06-014	level one	
07-054	to	06-054		
08-014	to	07-014	level two	
08-054	to	07-054		
06-014	to	05-014	level two to level one on five	
06-054	to	05-054		

09-015	to	08-015	level one	K13
09-055	to	08-055		
07-015	to	06-015	level one	
07-055	to	06-055		
08-015	to	07-015	level two	
08-055	to	07-055		
06-015	to	05-015	level two to level one on five	
06-055	to	05-055		

09-016	to	08-016	level one	K14
09-056	to	08-056		
07-016	to	06-016	level one	
07-056	to	06-056		
08-016	to	07-016	level two	
08-056	to	07-056		
06-016	to	05-016	level two to level one on five	
06-056	to	05-056		

Twisted Pairs				Signal Name
09-017	to	08-017	level one	K15
09-057	to	08-057		
07-017	to	06-017	level one	
07-057	to	06-057		
08-017	to	07-017	level two	
08-057	to	07-057		
06-017	to	05-017	level two to level one on five	
06-057	to	05-057		

08-023	to	07-023	level one	MOSP
08-063	to	07-063		
06-023	to	05-023	level one	
06-063	to	05-063		
09-099	to	08-023	level two	
09-059	to	08-063		
07-023	to	06-023	level two	
07-063	to	06-063		

08-104	to	07-104	level one	SEXCK1
08-065	to	07-065		
06-104	to	05-104	level one	
06-065	to	05-065		
09-104	to	08-104	level two	
09-064	to	08-065		
07-104	to	06-104	level two	
07-065	to	06-065		

08-025	to	07-025	level one	SEXCK23
08-026	to	07-026		
06-025	to	05-025	level one	
06-026	to	05-026		
09-102	to	08-025	level two	
09-062	to	08-026		
07-025	to	06-025	level two	
07-026	to	06-026		

Twisted Pairs				Signal Name
08-108	to	07-108	level one	R/$\overline{W}$
08-069	to	07-069		
06-108	to	05-108	level one	
06-069	to	05-069		
09-108	to	08-108	level two	
09-068	to	08-069		
07-108	to	06-108	level two	
07-069	to	06-069		

08-022	to	07-022	level one	$\overline{\text{MORE 23}}$
08-062	to	07-062		
06-022	to	05-022	level one	
06-062	to	05-062		
09-101	to	08-022	level two	
09-061	to	08-062		
07-022	to	06-022	level two	
07-062	to	06-062		

08-105	to	07-105	level one	$\overline{\text{MOSE 1}}$
08-066	to	07-066		
06-105	to	05-105	level one	
06-066	to	05-066		
09-105	to	08-105	level two	
09-065	to	08-066		
07-105	to	06-105	level two	
07-066	to	06-066		

08-024	to	07-024	level one	$\overline{\text{MOSE 23}}$
08-064	to	07-064		
06-024	to	05-024	level one	
06-064	to	05-064		
09-103	to	08-024	level two	
09-063	to	08-064		
07-024	to	06-024	level two	
07-064	to	06-064		

Twisted Pairs				Signal Name
08-106	to	07-106	level one	OVFG
08-067	to	07-067		
06-106	to	05-106	level one	
06-067	to	05-067		
09-106	to	08-106	level two	
09-066	to	08-067		
07-106	to	06-106	level two	
07-067	to	06-067		

08-089	to	07-089	level one	$\overline{\text{P2CLR}}$
08-090	to	07-090		
06-089	to	05-089	level one	
06-090	to	05-090		
09-083	to	08-089	level two	
09-043	to	08-090		
07-089	to	06-089	level two	
07-090	to	06-090		

08-084	to	07-084	level one	$\overline{\text{P3CLR}}$
08-085	to	07-085		
06-084	to	05-084	level one	
06-085	to	05-085		
09-084	to	08-084	level two	
09-044	to	08-085		
07-084	to	06-084	level two	
07-085	to	06-085		

08-088	to	07-088	level one	$\overline{\text{SACK DFM}}$
08-087	to	07-087		
06-088	to	05-088	level one	
06-087	to	05-087		
09-088	to	08-088	level two	
09-087	to	08-087		
07-088	to	06-088	level two	
07-087	to	06-087		

Twisted Pairs				Signal Name
08-103	to	07-103	level one	$\overline{\text{P4CLR}}$
08-102	to	07-102		
06-103	to	05-103	level one	
06-102	to	05-102		
09-085	to	08-103	level two	
09-045	to	08-102		
07-103	to	06-103	level two	
07-102	to	06-102		

08-082	to	07-082	level one	$\overline{\text{P1CLR}}$
08-083	to	07-083		
06-082	to	05-082	level one	
06-083	to	05-083		
09-082	to	08-082	level two	
09-042	to	08-083		
07-082	to	06-082	level two	
07-083	to	06-083		

08-109	to	07-109	level one	$\overline{\text{MIRE 1}}$
08-110	to	07-110		
06-109	to	05-109	level one	
06-110	to	05-110		
09-109	to	08-109	level two	
09-069	to	08-110		
07-109	to	06-109	level two	
07-110	to	06-110		

08-021	to	07-021	level one	$\overline{\text{MIRE 23}}$
08-020	to	07-020		
06-021	to	05-021	level one	
06-020	to	05-020		
09-100	to	08-021	level two	
09-060	to	08-020		
07-021	to	06-021	level two	
07-020	to	06-020		

Twisted Pairs				Signal Name
08-107	to	07-107	level one	$\overline{\text{MORE 1}}$
08-068	to	07-068		
06-107	to	05-107	level one	
06-068	to	05-068		
09-107	to	08-107	level two	
09-067	to	08-068		
07-107	to	06-107	level two	
07-068	to	06-068		
08-091	to	07-091	level one	$\overline{\text{DFM CLR}}$
08-092	to	07-092		
06-091	to	05-091	level one	
06-092	to	05-092		
09-093	to	08-091	level two	
09-092	to	08-092		
07-091	to	06-091	level two	
07-092	to	06-092		

#26 Wires

Slot 9, 8, 7, 6, 5:

IO 40, 80, 120

Gnd: 1 wire from each

IO 1, 41, 81

+5V: 1 wire from each

Single #30 Wires

08-031	to	07-031	level one	ADDR 0
06-031	to	05-031	level one	
09-071	to	08-031	level two	
07-031	to	06-031	level two	
08-032	to	07-032	level one	ADDR 1
06-032	to	05-032	level one	
09-072	to	08-032	level two	
07-031	to	06-031	level two	

Single #30 Wires				Signal Name
08-033	to	07-033	level one	ADDR 2
06-033	to	05-033	level one	
09-073	to	08-033	level two	
07-033	to	06-033	level two	

08-034	to	07-034	level one	ADDR 3
06-034	to	05-034	level one	
09-114	to	08-034	level two	
07-034	to	06-034	level two	

08-035	to	07-035	level one	ADDR 4
06-035	to	05-035	level one	
09-075	to	08-035	level two	
07-035	to	06-035	level two	

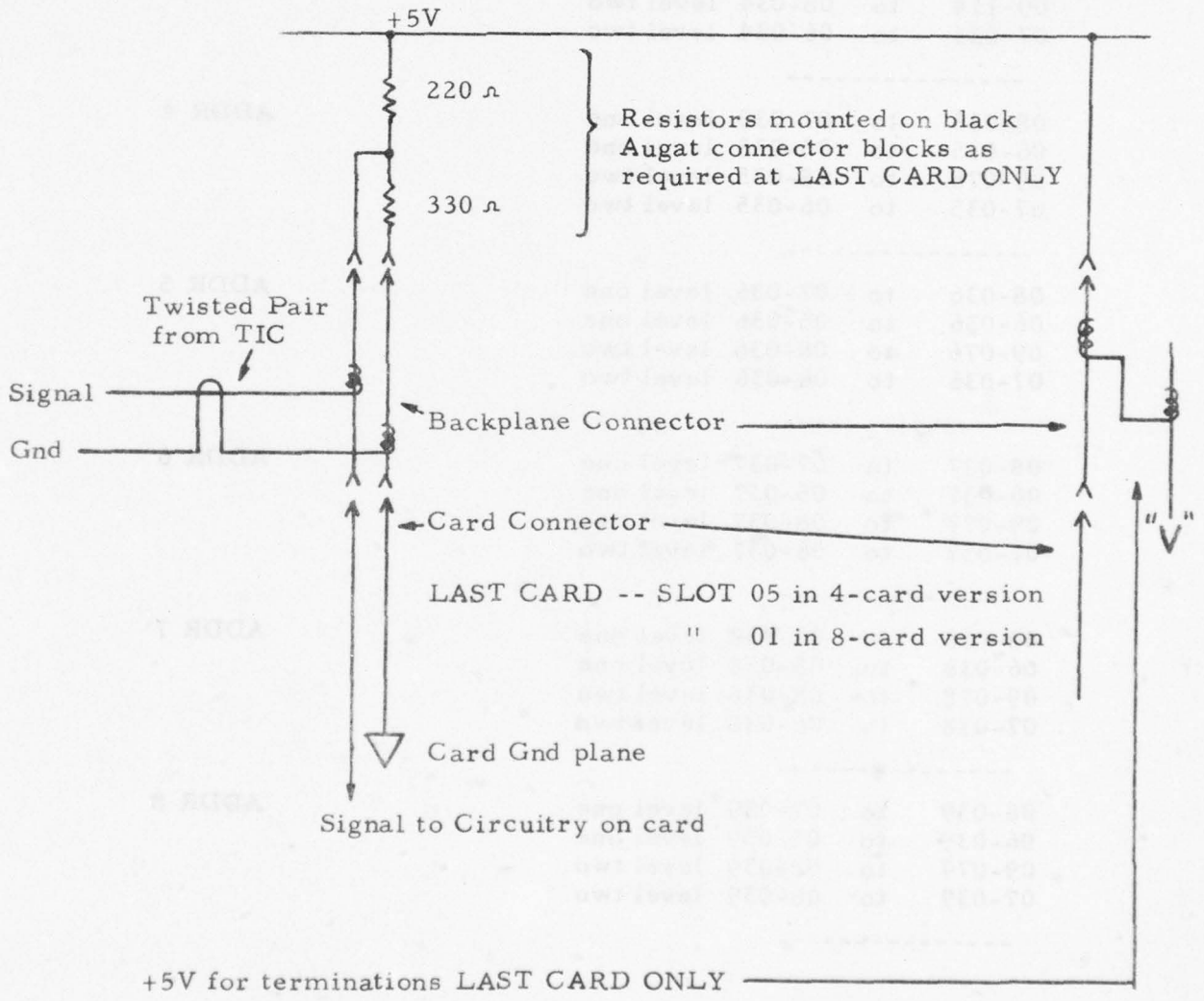
08-036	to	07-036	level one	ADDR 5
06-036	to	05-036	level one	
09-076	to	08-036	level two	
07-036	to	06-036	level two	

08-037	to	07-037	level one	ADDR 6
06-037	to	05-037	level one	
09-077	to	08-037	level two	
07-037	to	06-037	level two	

08-038	to	07-038	level one	ADDR 7
06-038	to	05-038	level one	
09-078	to	08-038	level two	
07-038	to	06-038	level two	

08-039	to	07-039	level one	ADDR 8
06-039	to	05-039	level one	
09-079	to	08-039	level two	
07-039	to	06-039	level two	

Termination of each Twisted Pair from TIC



Cable:T Backplane to Canceller Interface (CI) Connector
on top of PPP20 card in slot F7

Twisted Pairs -Cable			Color	Signal Name
CI-007	to		Wh	Spare
CI-008	to		Brn	
CI-010	to		Pur	Spare
CI-011	to		Blk	
CI-012	to		Pur	Spare
CI-013	to		Blk	
CI-014	to	09-034	Pur	∅3LB
CI-015	to	09-074	Blk	
CI-016	to	09-032	Pur	$\overline{\text{ACX}}$
CI-017	to	09-033	Blk	
CI-018	to	09-018	Wh	ORL
CI-019	to	09-019	Brn	
CI-020	to	09-020	Wh	$\overline{\text{PISOR RE}}$
CI-021	to	09-021	Brn	
CI-022	to	09-022	Wh	$\overline{\text{SRE}}$
CI-023	to	09-023	Brn	
CI-024	to	09-024	Wh	$\overline{\text{SACK B}}$
CI-025	to	09-025	Brn	
CI-026	to	09-026	Wh	PISOR SP
CI-027	to	09-027	Brn	
CI-028	to	09-028	Wh	e_{in} GATE
CI-029	to	09-029	Brn	
CI-082	to	08-100	Brn	e_{out}0Q
CI-083	to	08-101	Blk	
CI-084	to	08-098	Wh	e_{in}0Q
CI-085	to	08-099	Blk	
CI-086	to	07-100	Gray	e_{out}0I
CI-087	to	07-101	Blk	
CI-088	to	07-098	Pur	e_{in}0I
CI-089	to	07-099	Blk	
CI-090	to	06-100	Blu	e_{out}1Q
CI-091	to	06-101	Blk	
CI-092	to	06-098	Grn	e_{in}1Q
CI-093	to	06-099	Blk	

Twisted Pairs -Cable			Color	Signal Name
CI-094	to	05-100	Yel	e_{out} 1I
CI-095	to	05-101	Blk	
CI-096	to	05-098	Or	e_{in} 1I
CI-097	to	05-099	Blk	
CI-098	to		Red	e_{out} 2Q
CI-099	to		Blk	
CI-100	to		Brn	e_{in} 2Q
CI-101	to		Blk	
CI-102	to		Brn	e_{out} 2I
CI-103	to		Blk	
CI-104	to		Wh	e_{in} 2I
CI-105	to		Blk	
CI-106	to		Gray	e_{out} 3Q
CI-107	to		Blk	
CI-108	to		Pur	e_{in} 3Q
CI-109	to		Blk	
CI-110	to		Blu	e_{out} 3I
CI-111	to		Blk	
CI-112	to		Grn	e_{in} 3I
CI-113	to		Blk	
CI-114	to		Yel	Spare
CI-115	to		Blk	
CI-116	to		Or	Spare
CI-117	to		Blk	
CI-118	to		Red	Spare
CI-119	to		Blk	
CI-120	to		Brn	Spare
CI-080	to		Blk	

Single Wires - Cable			
CI-001	TG plane	Wh	Gnd
CI-002		Brn	Spare
CI-003	TG plane	Wh	Gnd
CI-004		Brn	Spare
CI-005	TG plane	Wh	Gnd
CI-006		Brn	Spare

Single Wires - Cable		Color	Signal Name
CI-009	TG plane	Wh	Gnd
CI-030	to 09-030	Wh	DLOE
CI-031	to 09-031	Brn	CG
CI-032	to 09-090	Wh	CLK WIDTH
CI-033	to 09-091	Wh	CLK WIDTH
CI-034	to	Wh	Spare
CI-035	to 09-035	Wh	CSA
CI-036	to 09-036	Wh	CSB
CI-037	to 09-037	Wh	CSC
CI-038	to 09-038	Wh	CG--ON
CI-039	TG plane	Wh	Gnd
CI-040	TG plane	Wh	Gnd

APPENDIX B

"PPP Canceller Constants", memo AJJ-58

RAYTHEON

FORM 10-0557 (9-65) BOND

DIVISION EQUIPMENT
Operation EDL
Department ADL - Wayland

Classification Unclassified

Contract No. F19628-76-C-0297

Distribution cc

File No. -

Memo No. AJJ-58

Date 31 January 1977

To H. L. Groginsky

From A. J. Jagodnik, Jr.

Subject PPP Canceller Constants

The radar system parameters necessary to specify the eight sets of constants for the PPP Ground Clutter Canceller have been established as listed in Table 1 (attached). The bold-face numbers under each PRF/radar frequency combination represent AFGL requirements per our 77 Jan. 31 meeting. By chance, one set of constants, "G" in the table, satisfied two AFGL requirements. I therefore took the liberty of specifying the extra constant to give a 0.16 meters/sec. cut-off at the highest Porcupine PRF. With this arrangement, notch width increases monotonically as the CANCELLER SHAPE switch is rotated clockwise and a useful range of widths is available at each PRF.

A. J. Jagodnik, Jr.
Advanced Electronic Techniques
Wayland Box M9, x5171

AJJ/lld

cc: G. Armstrong AFGL
A. Bishop "
K. M. Glover "
A. L. Glick

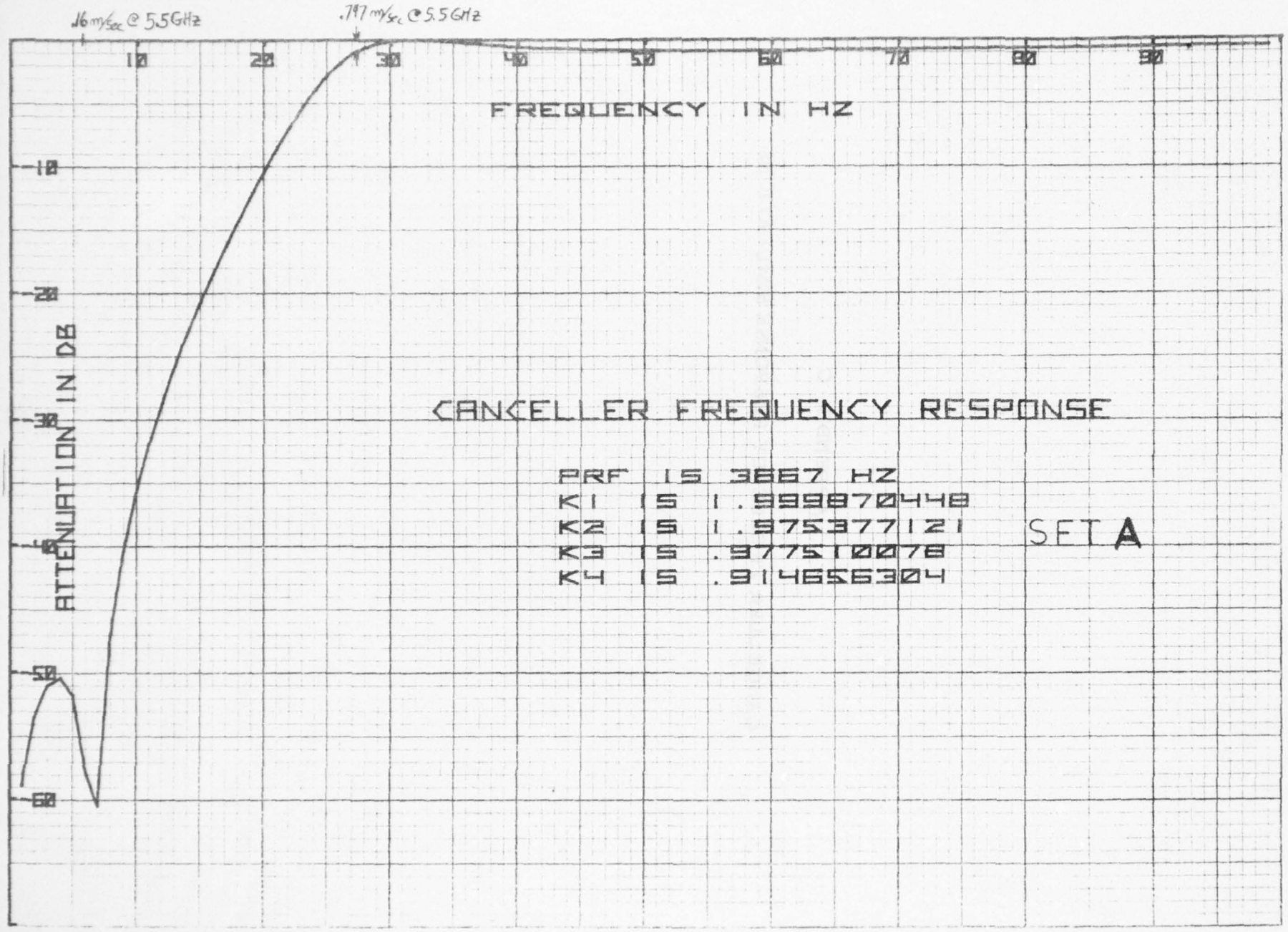
Table 1.

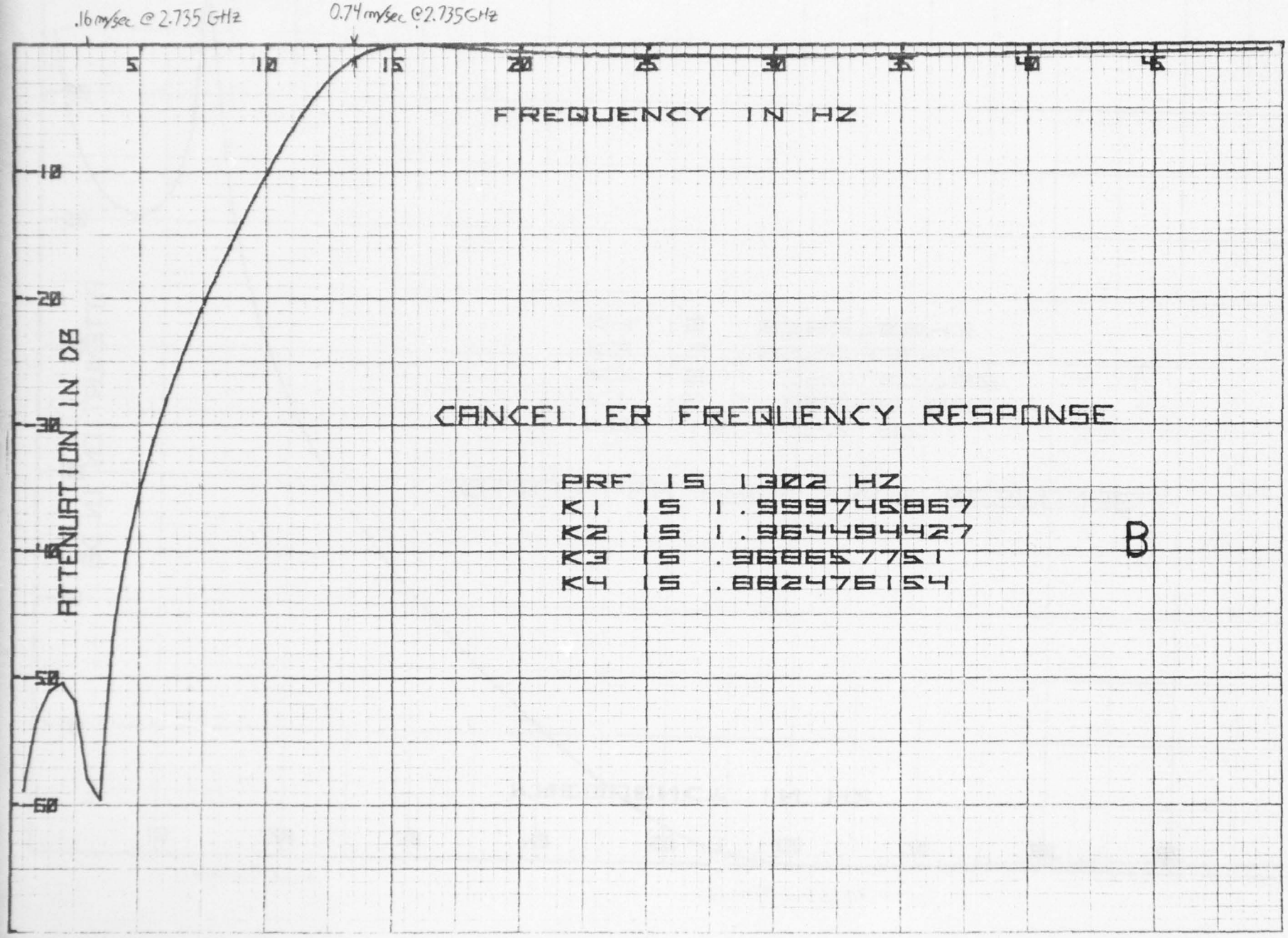
"CANCELLER SHAPE" SWITCH POS:	RADAR FREQ PRF f_r (Hz) $2f_c/f_r$ (x10^{-3}) ①	PORCUPINE - 5500 MHz					CIMMARON 2735 MHz	
		458	917	1222	1833	3667	456	1302
		VELOCITY CUT-OFF (m/sec)						
A	3.199709	.02	.04	.0533	.08	.16	.04	.1142
B	4.481311	.0280	.0560	.0746	.1120	.2240	.0560	.16
C	6.399418 (2A)	.04	.08	.1066	.16	.32	.08	.2285
D	8.962622 (2B)	.0560	.1120	.1493	.2241	.4482	.1120	.32
E	12.80233 (2C)	.08	.16	.2133	.32	.64	.16	.4569
F	19.20349 (1.5E)	.12	.24	.32	.48	.96	.24	.6855
G	25.59069 (2E)	.16	.32	.4266	.64	1.28	.32	.9140
H	51.23726 (2G)	.32	.64	.8533	1.28	2.56	.64	1.828

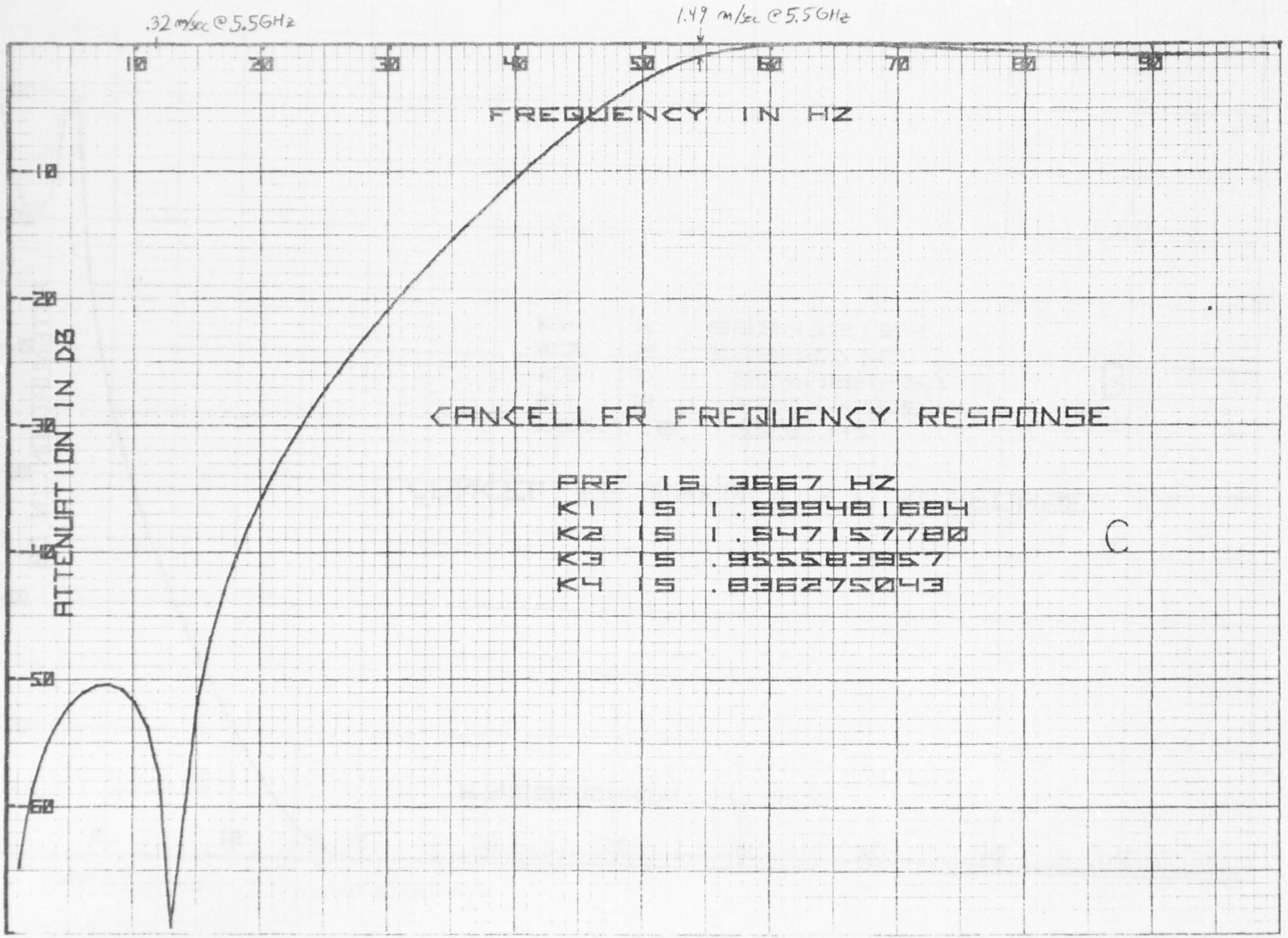
① Ratio of the cutoff Frequency f_c to the maximum unambiguous doppler Frequency.

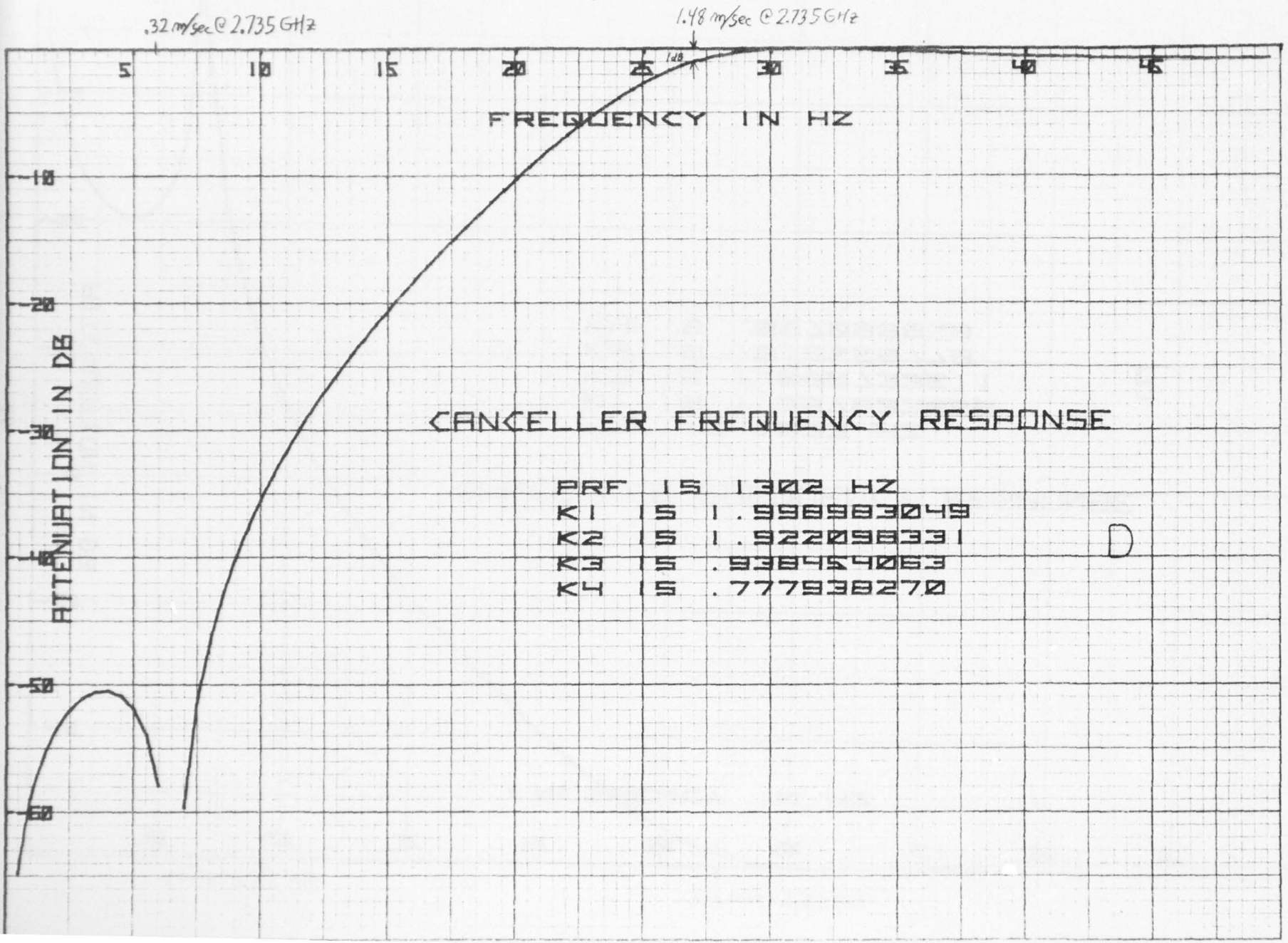
APPENDIX C

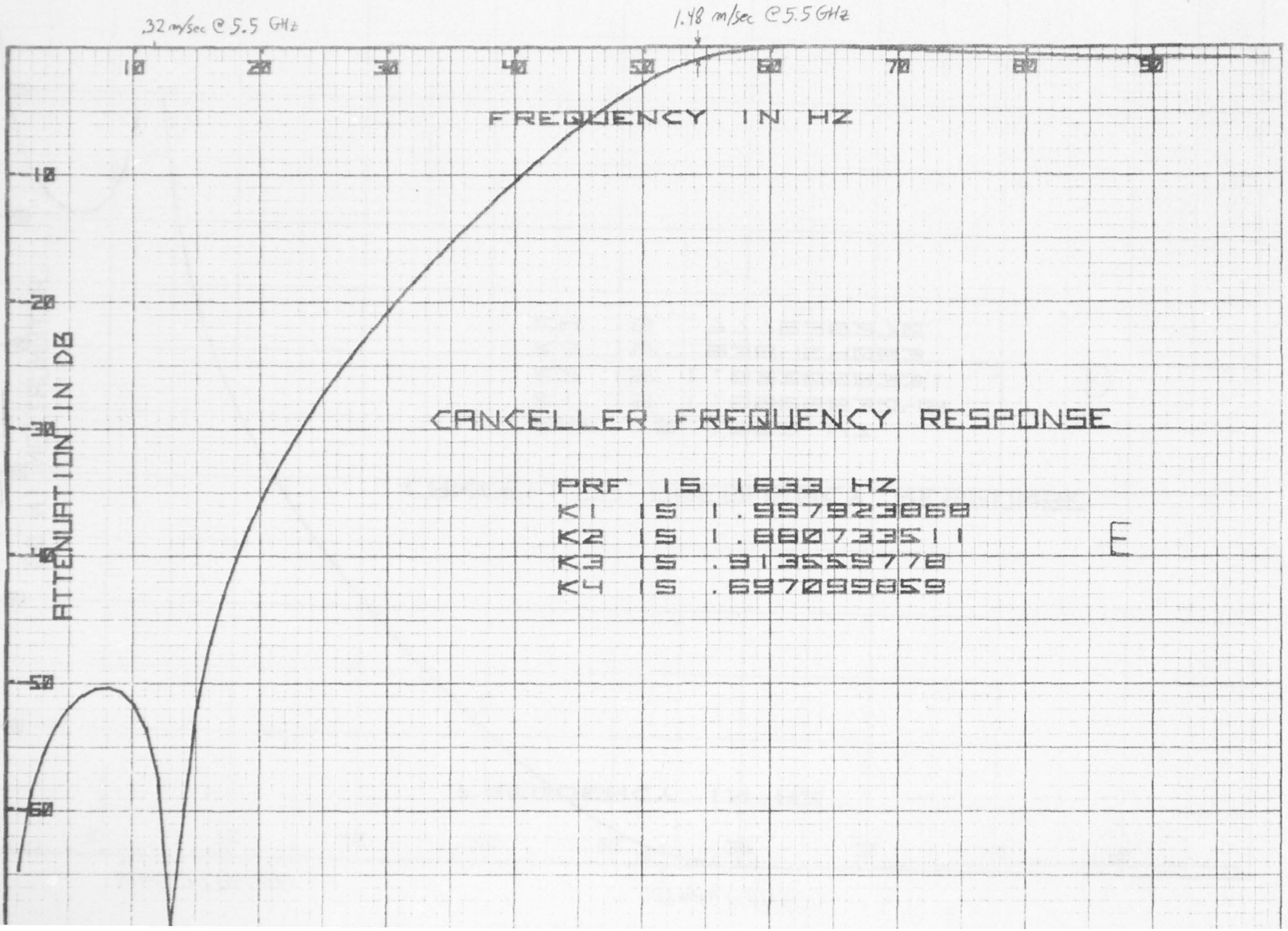
CANCELLER FREQUENCY RESPONSE SIMULATIONS



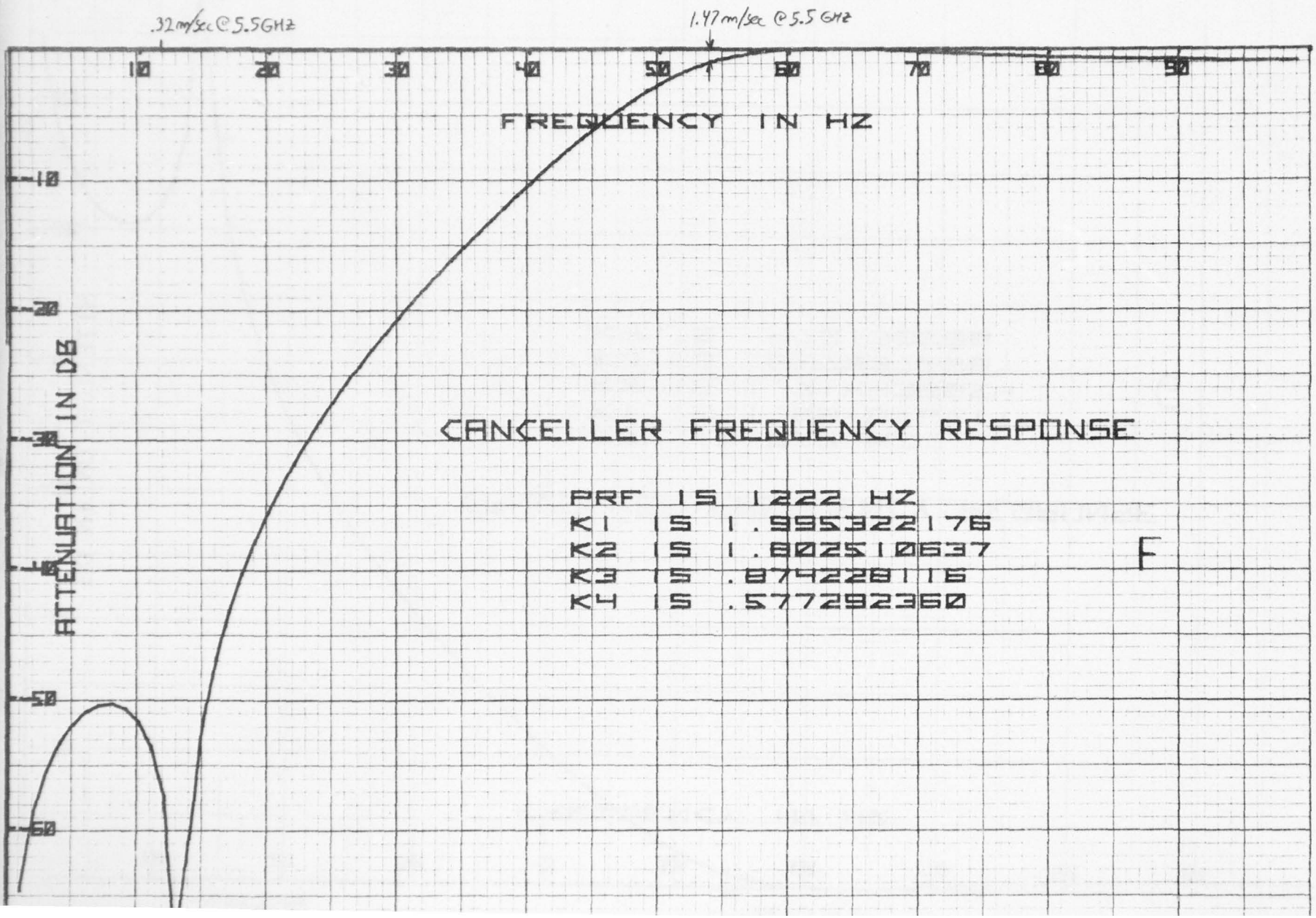


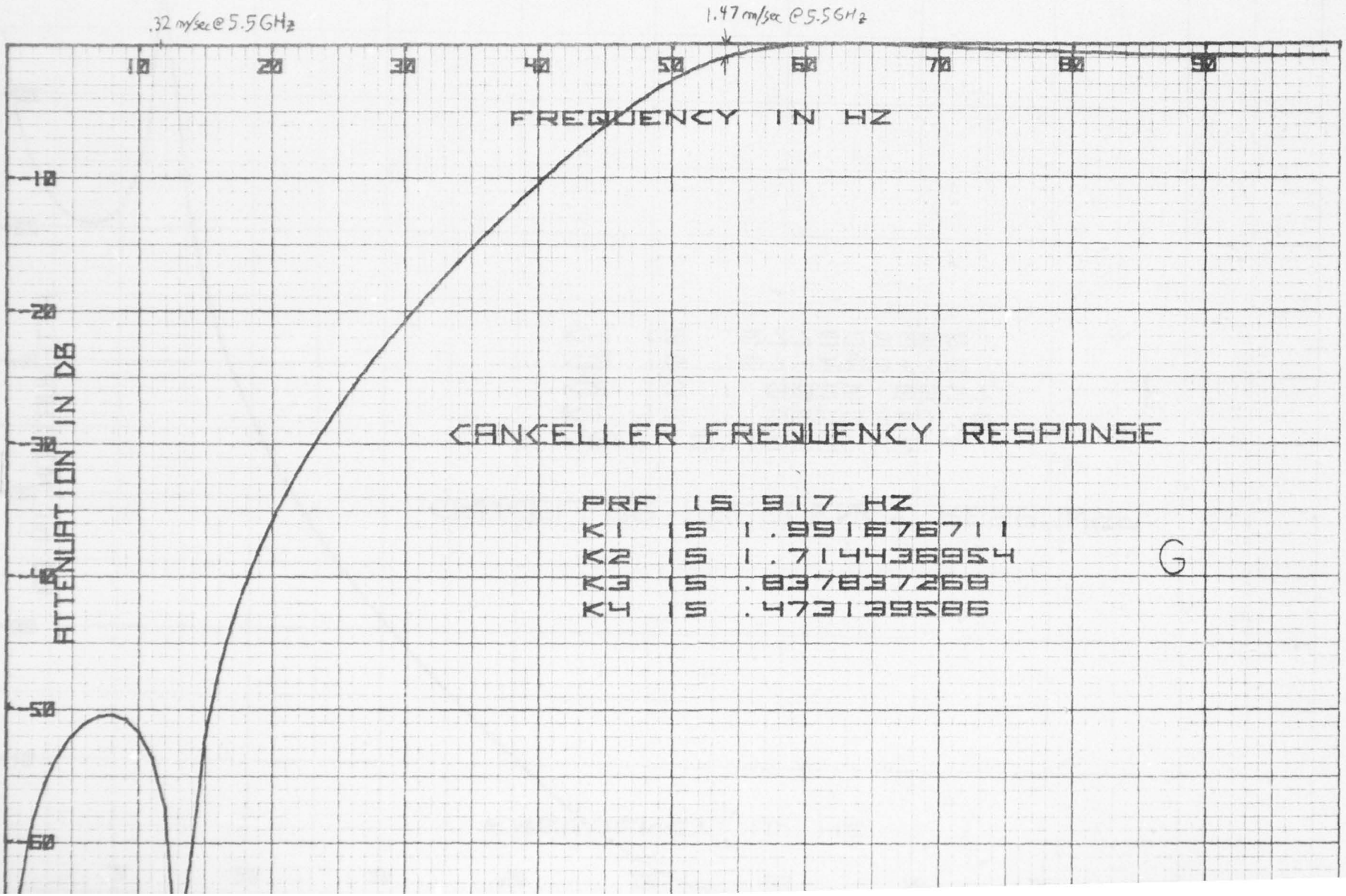




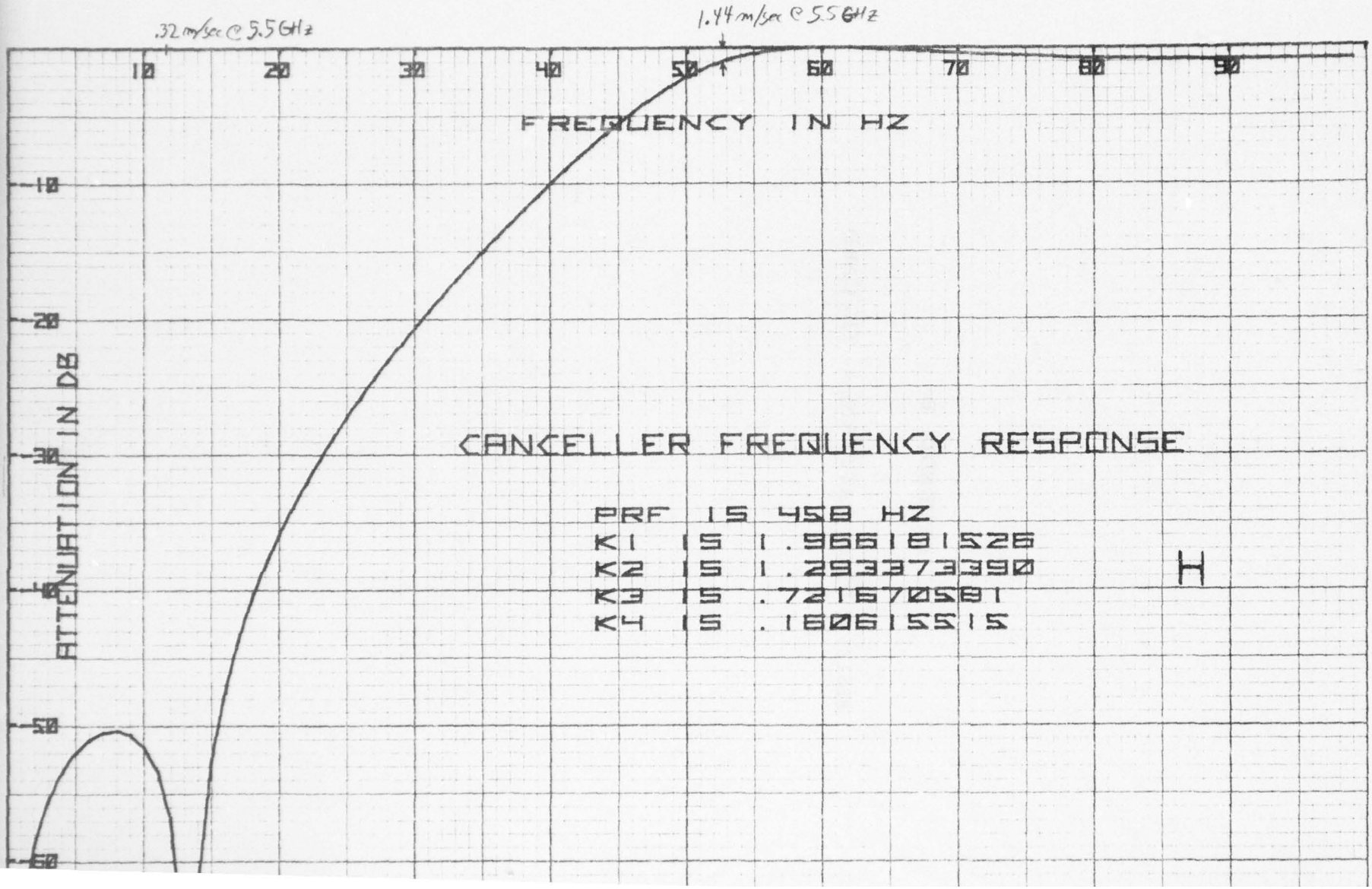


06


.32 m/sec @ 5.5 GHz
1.47 m/sec @ 5.5 GHz
10
20
30
40
50
60
70
80
90
FREQUENCY IN HZ
-10
-20
-30
-40
-50
-60
ATTENUATION IN DB
CANCELLER FREQUENCY RESPONSE
PRF IS 1222 HZ
K1 IS 1.995322176
K2 IS 1.802510637
K3 IS .874228116
K4 IS .577292360
F


.32 m/sec @ 5.5 GHz
1.47 m/sec @ 5.5 GHz
10
20
30
40
50
60
70
80
90
FREQUENCY IN HZ
10
20
30
40
50
60
ATTENUATION IN DB
CANCELLER FREQUENCY RESPONSE
PRF IS 917 HZ
K1 IS 1.991676711
K2 IS 1.714436954
K3 IS .837837268
K4 IS .473139586
G

H 9



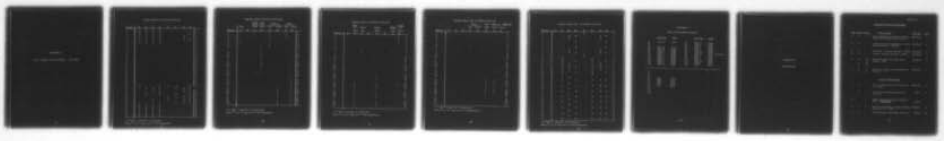
APPENDIX D

82S123 K PROM PATTERNS -- TIC CARD

SHAPE SWITCH	PROM ADDR	CONST	B7 1111 5432	R26 11 1098	B7 7654	T26 3210		CO TO
A	00	K4	...H	.H.H	HH.H	H...	K4	.
	01	K3	....	.H.H	HH..	...H	K3	.
	02	K2/2	....	..HH	..H.	.HH.	K2	1.
	03	K1/2	....	....	....	..HH	K1	1.
B	04	K4	...H	HHH.	...H	.H.H	K4	.
	05	K3	....	H...	....	.H.H	K3	.
	06	K2/2	....	.H..	H...	H.H.	K2	1.
	07	K1/2	....	....	....	.HHH	K1	1.
C	08	K4	..H.	H..H	HHH.	H..H	K4	.
	09	K3	....	H.HH	.H.H	HHH.	K3	.
	10	K2/2	....	.HH.	HH..	..HH	K2	1.
	11	K1/2	....	....	...H	....	K1	1.
D	12	K4	..HH	H...	HH.H	H...	K4	.
	13	K3	....	HHHH	HH..	....	K3	.
	14	K2/2	....	H..H	HHHH	H...	K2	1.
	15	K1/2	....	....	..H.	....	K1	1.
E	16	K4	.H..	HH.H	H...	H.H.	K4	.
	17	K3	...H	.HH.	..H.	....	K3	.
	18	K2/2	....	HHHH	.H..	..HH	K2	1.
	19	K1/2	....	....	.H..	..HH	K1	1.
F	20	K4	.HH.	HH..	..HH	.HH.	K4	.
	21	K3	..H.	....	..HH	..H.	K3	.
	22	K2/2	...H	H..H	.H..	.HH.	K2	1.
	23	K1/2	....	....	H..H	H...	K1	1.
G	24	K4	H...	.HH.	HH.H	HHHH	K4	.
	25	K3	..H.	H..H	H...	..H.	K3	.
	26	K2/2	..H.	.H..	H...	HH..	K2	1.
	27	K1/2	....	...H	...H	....	K1	1.
H	28	K4	HH.H	.HH.	HHH.	...H	K4	.
	29	K3	.H..	.HHH	.H..	....	K3	.
	30	K2/2	.H.H	H.H.	.HHH	..H.	K2	1.
	31	K1/2	....	.H..	.H.H	..HH	K1	1.

AD-A045 589 RAYTHEON CO WAYLAND MASS ADVANCED DEVELOPMENT LAB F/G 17/9
R AND D EQUIPMENT INFORMATION REPORT. VOLUME I. WEATHER RADAR T--ETC(U)
APR 77 R K VANDERKRUIK, A J JAGODNIK F19628-76-C-0297
UNCLASSIFIED ER77-4128 AFGL-TR-77-0171 NL

2 OF 2
AD A045589



END
DATE FILMED
11-77
DDC

APPENDIX E

82S123 TIMING PROM PATTERNS -- TIC CARD

Signetics 82S123, U35 (L26) on TIC Card

Address	B7	B6	B5	B4	B3	B2	B1	B0	
0	H	H	H	H					0
1	H	H	H	H				H	1
2	H	H	H	H			H		2
3	H	H	H	H			H	H	3
4	H	H	H	H					4
5									5
6									6
7									7
8									8
9									9
10									10
11									11
12									12
13									13
14									14
15									15
16									16
17									17
18									18
19									19
20	H			H	H	H		H	20
21		H	H	H		H	H	H	21
22			H	H			H	H	22
23		H		H		H		H	23
24					H	H	H	H	24
25			H		H		H	H	25
26				H		H	H	H	26
27	H	H	H	H					27
28	H	H	H	H					28
29	H	H	H	H					29
30	H	H	H	H					30
31	H	H	H	H					31

H ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Signetics 82S123, U36 (J26) on TIC Card

			$\overline{\text{MORE}}$1	$\overline{\text{R/W}}$	MIRE 23		MIRE 1		
	ORL		Early	Early	Late	Early	Late	Early	
Address	B7	B6	B5	B4	B3	B2	B1	B0	
0			1		1		1		0
1					1		1		1
2		1			1		1		2
3					1				3
4	1				1				4
5					1				5
6				1	1				6
7				1					7
8				1					8
9				1					9
10				1					10
11				1					11
12				1					12
13				1					13
14				1					14
15				1					15
16				1					16
17			1	1					17
18			1						18
19								1	19
20								1	20
21								1	21
22								1	22
23						1		1	23
24						1		1	24
25						1		1	25
26						1		1	26
27						1		1	27
28						1		1	28
29						1		1	29
30						1		1	30
31						1		1	31

1 ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Signetics 82S123, U37 (G26) on TIC Card

Address	B7	MOSE 23 Early B6	OVFG Late B5	B4	MOSE 1 Early B3	B2	$\overline{\text{MOSP}}$ Late B1	$\overline{\text{MORE}}$ 23 Early B0	
0								1	0
1								1	1
2								1	2
3								1	3
4									4
5									5
6			1						6
7			1				1		7
8									8
9									9
10									10
11									11
12									12
13									13
14									14
15									15
16									16
17					1				17
18					1				18
19					1				19
20		1			1			1	20
21		1			1			1	21
22		1			1				22
23		1			1				23
24		1			1				24
25		1			1				25
26		1			1				26
27		1			1				27
28		1			1				28
29		1			1				29
30		1			1				30
31		1			1				31

1 ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Signetics 82S123 (3S), U38 (E26) on TIC Card

				RWCD		SRE	PISOR RE		$\overline{\text{PISOR SP}}$
				Late	Early	Early	Early	Early	
Address	B7	B6	B5	B4	B3	B2	B1	B0	
0									0
1									1
2									2
3									3
4									4
5									5
6				1					6
7									7
8									8
9									9
10									10
11									11
12									12
13									13
14									14
15									15
16							1	1	16
17									17
18					1				18
19						1			19
20						1	1		20
21						1	1		21
22						1	1		22
23						1	1		23
24						1	1		24
25						1	1		25
26						1	1		26
27									27
28									28
29									29
30									30
31									31

1 ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

Signetics 82S123 (3S), U54 (N44) on TIC Card

Address	B7	B6	B5	B4	B3	B2	B1	B0	
0					H				0
1			H	H			H	H	1
2			H				H		2
3				H				H	3
4									4
5				H				H	5
6			H				H		6
7			H	H			H	H	7
8					H				8
9		H				H			9
10		H		H		H		H	10
11		H	H			H	H		11
12		H	H	H		H	H	H	12
13		H	H			H	H		13
14		H		H		H		H	14
15		H				H			15
16			H						16
17		H		H		H	H	H	17
18			H						18
19		H		H		H	H	H	19
20			H						20
21		H		H		H	H	H	21
22			H						22
23		H		H		H	H	H	23
24			H						24
25		H		H		H	H	H	25
26			H						26
27		H		H		H	H	H	27
28			H						28
29		H		H		H	H	H	29
30			H						30
31		H		H		H	H	H	31

H ≡ High ≡ Logic One ≡ Programmed

Blank ≡ Low ≡ Logic Zero ≡ Not Programmed

APPENDIX F

PPP CARD INDEXING SUMMARY

	Card Type	Index		Card Type	Index	
R1	PPP-13	A3B7	F1	PPP-13	A3B7	
R2			F2	PPP-6	A8B5	
R3			F3	PPP-3	A6B4	
R4	PPP-3A	A6B5	F4	PPP-2	A8B8	
R5	PPP-9	A5B4	F5	PPP-2	A8B8	
R6	PPP-10	A4B4	F6	PPP-4A	A8B6	
R7	PPP-5	A7B4	F7	PPP-20	A7B3	Top-A1B3
R8	PPP-3	A6B4	F8	PPP-2	A8B8	
R9	PPP-3	A5B4	F9	PPP-1	A8B7	
R10	PPP-10	A4B4	F10	PPP-1	A8B7	
R11	PPP-3	A6B4	F11	PPP-2A	A4B8	
R12	PPP-9	A5B4	F12	PPP-8	A8B1	
R13	PPP-10	A4B4	F13	PPP-7	A8B2	

T1		
T2		
T3		
T4		
T5	DFM	A1B1
T6	DFM	A1B1
T7	DFM	A1B1
T8	DFM	A1B1
T9	TIC	A1B2
T10		
T11		
T12		
T13		

APPENDIX G

DRAWING LIST

TRACAN PPP Canceller Drawings

Size	Form	No. Sht.	New Drawings	Dwg. No.	Rev.
C	V	1	Power Supply Interconnection Schematic, Pulse Pair Processor with Canceller	SD192634	A
D	S	1	Layout and Schematic Additions -- Scale Card with Delay -- PPP3A	SD192635	A
E	V	1	Schematic - Canceller Interface - PPP20	SD192636	A
D	S	1	Layout - Canceller Interface - PPP20	SD192637	A
D	V	1	Schematic and Layout Digital Filter Module - DFM	SD192638	A
	S	4			
D	V	1	Schematic and Layout Timing Interface Controller - TIC	SD192639	A
	S	1			

Revised PPP Drawings

E	S	1	Electrical Schematic-AGC Accumulator Card- PPP 6	SD895169	B
J	S	1	Interconnection Diagram Pulse Pair Processor	895171	C
D		1	Power Supply Interconnection Diagram PPP -- OBSOLETE	895157	
E	S	1	Electrical Schematic - Timing and Dump Generator Card - PPP5	SD895162	B
D	V	1	Block Diagram of Pulse Pair Processor	895155	B